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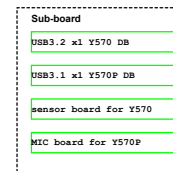
Yx70 GN20E M/B Schematics Document

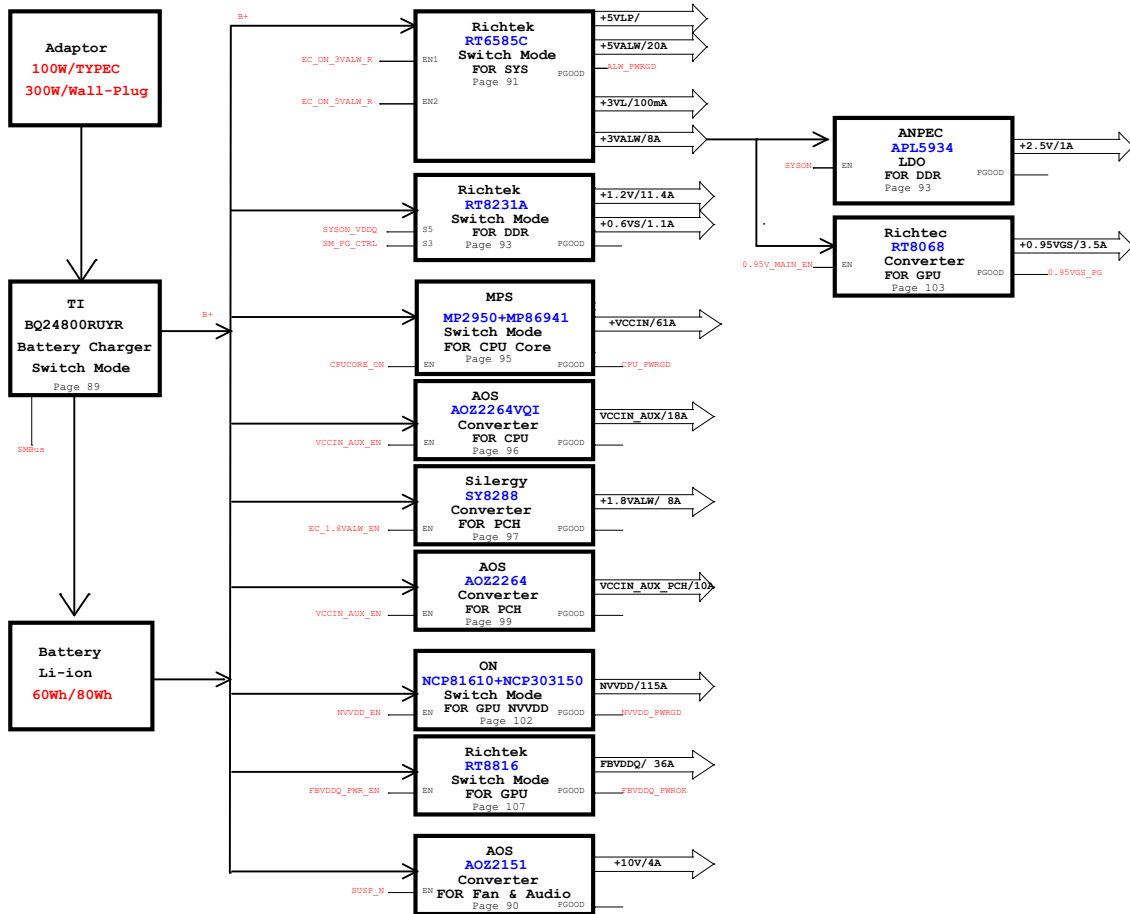
Alder Lake P-Processor with DDR5 + NV GN20-E GPU

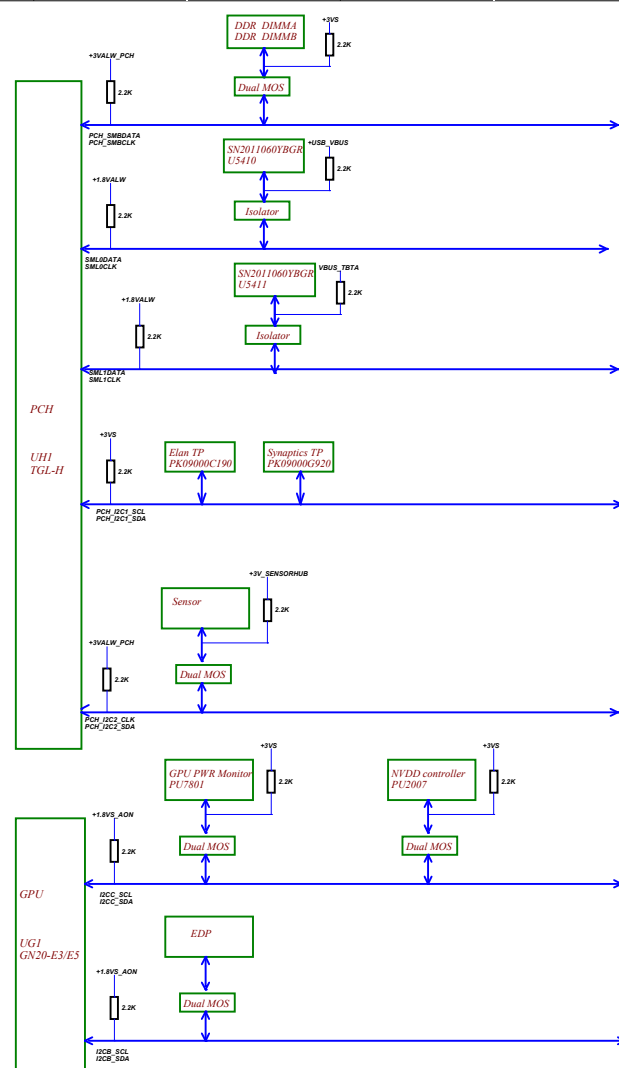
2021-11-29

REV: A0

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			Custom	y550	A0
			Date:	Monday, November 29, 2021	Sheet 1 of 110







SMBUS Control Table

GN20x-E GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVDD_PWM_VID	PWM Output to control NVDD	NVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN	(10K PD)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K PU)
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL	(10K PD)
GPIO4	OUT	MSVDD_EN	GPU power sequencing for GC6 --MSVDD_EN	GPIO4_GC6_MSVDD_EN	(10K PU)
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVDD_PSI*	Phase Shedding, NVDD_PSI	NVDD_PSI	(10K PU) RSVD
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K PD)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K PD)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K PU)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL	(100K PD)
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_ENVDD	(10K PD)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K PU)
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	IGPU_EDP_ENBK_L	(100K PU)
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K PU)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	IFPB_HPD	(10K PU)
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT	(10K PD)
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_HPD	(10K PU)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	UNUSED	
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBK_L	(100K PD)
GPIO22	OUT	ADC_MUX_SEL	OVRM MUX Input SEL	ADC_MUX_SEL	(2.2K PU)
GPIO23	OUT	UNUSED			
GPIO24	IN	HPD_IFPF*/USBC_HPD* or DONGLE_DET*	Hot Plug Detect for IFPF or USBC	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	(5.1K PU)
GPIO26	OUT	ROM_WP* FP_FUSE N18P-G61-A Control FP_FUSE	Connect to WP pin of the GPU EEPROM	GPIO26_ROM_WP GPIO26_FP_FUSE	(10K PD) (10K PD) RSVD
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K PU)
GPIO28	OUT	MSVDD_PWM_VID	PWM Ooutput to CNTL MSVDD	UNUSED	
GPIO29	OUT	NVDD_EN	NVDD Enable RSVD	GPIO29_NVDD_EN	(100K PU) RSVD
GPIO30	OUT	MSVDD_PSI*	Phase Shedding	UNUSED	

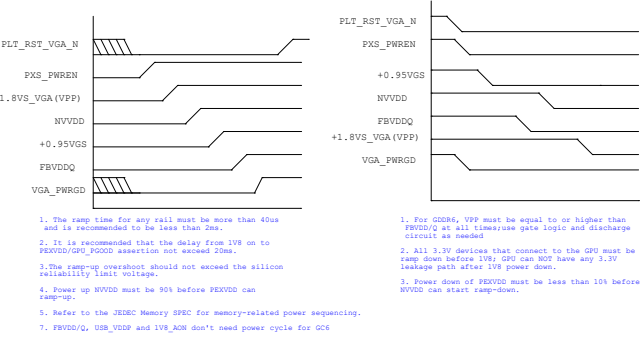
H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	GN20x-E VRAM
L	L	L	0 (0x0000)	Samsung K4Z803258C-HC14
L	L	H	1 (0x0001)	Micron MT61H256M32JE-14-A
L	H	L	2 (0x0002)	Hynix H56C8H24AIR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	Samsung (or E7) K4ZAF3258M-HC 14
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

FS_OVERT# FUNCTION

ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT# FUNCTION
L	L	H	FS_OVERT# function ENABLE
L	L	L	FS_OVERT# function DISABLE Reserved, do not configure


GN20x-E Power Sequence

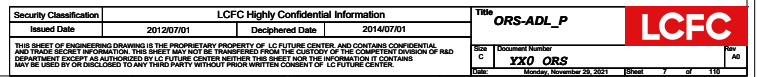


STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

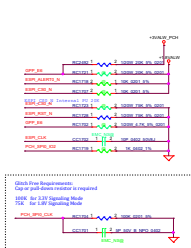
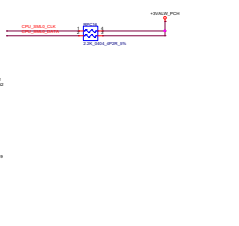
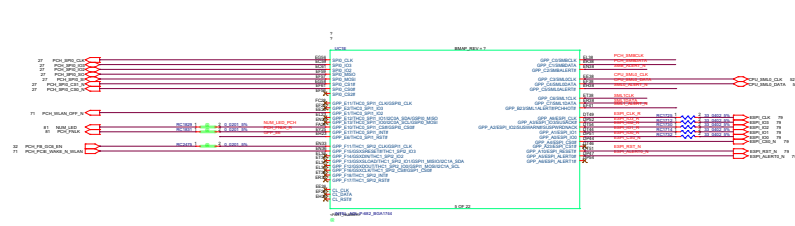
- 1:SMB_ALT_ADDR ENABLE
- 0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
- 0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
- 0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
- 0:VGA_DEVICE DISABLE

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File	Memory	Version	25/2021	Printed 5 of 116

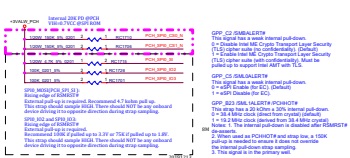
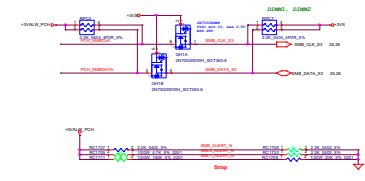
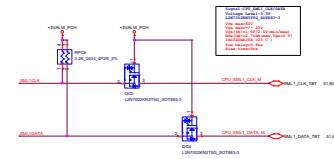
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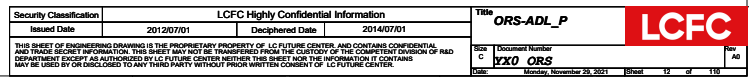


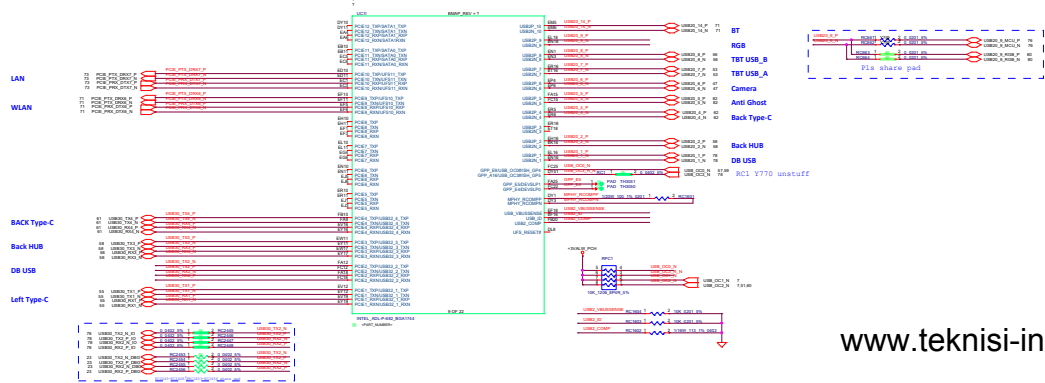




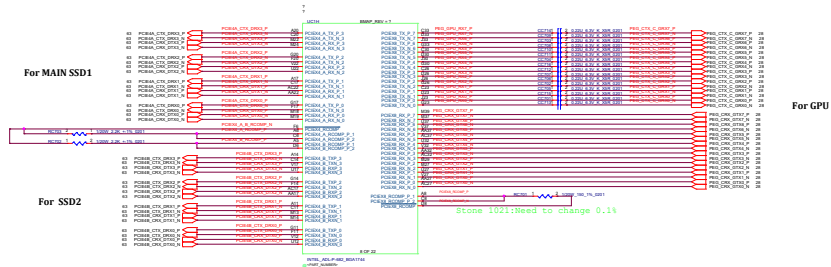
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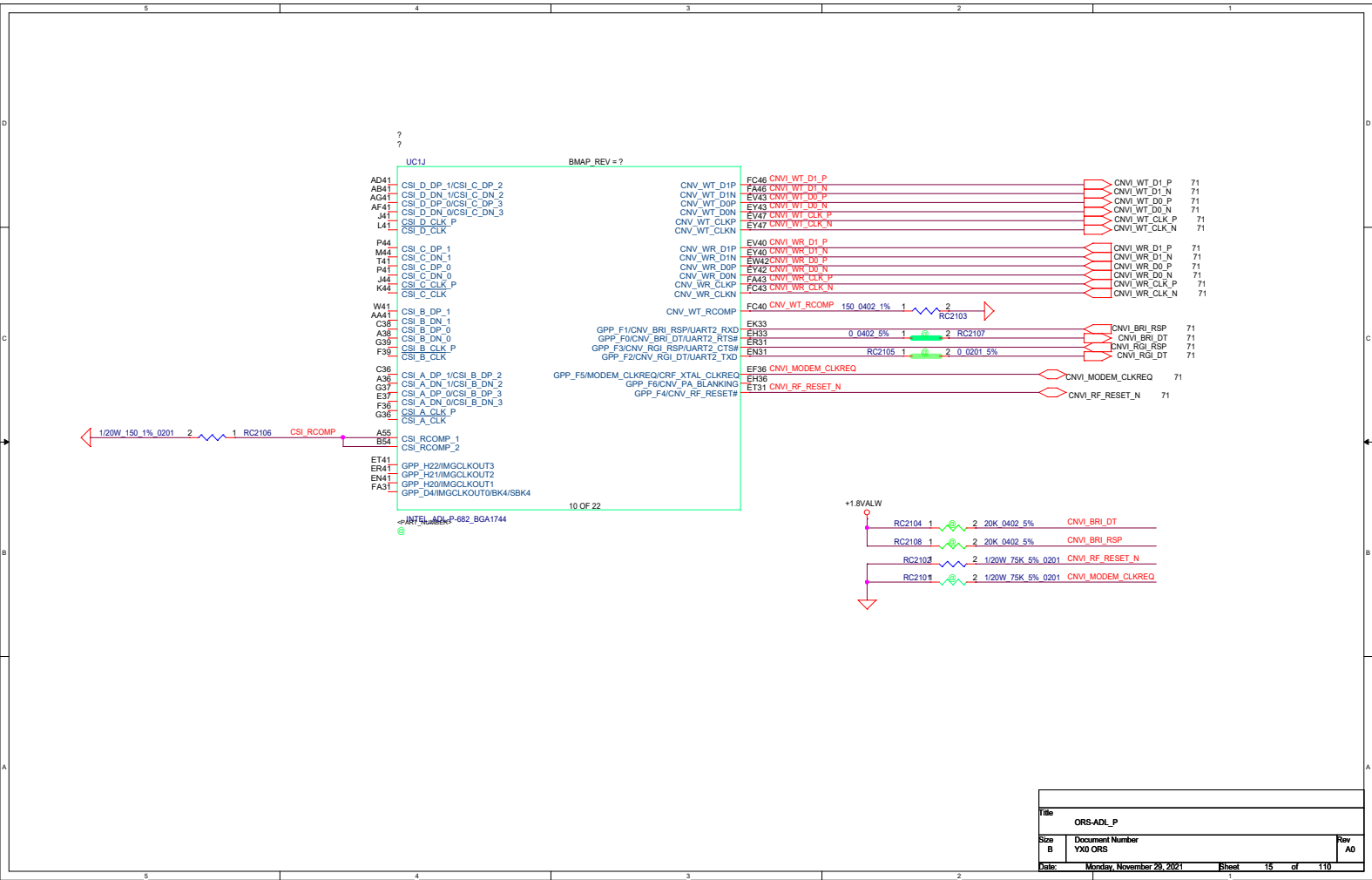





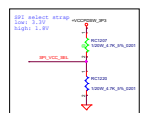
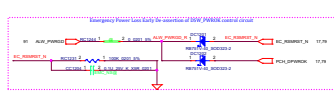
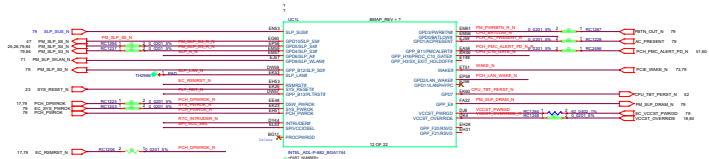


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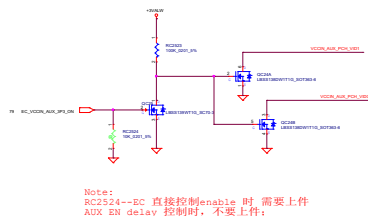




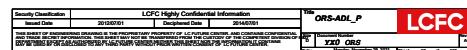
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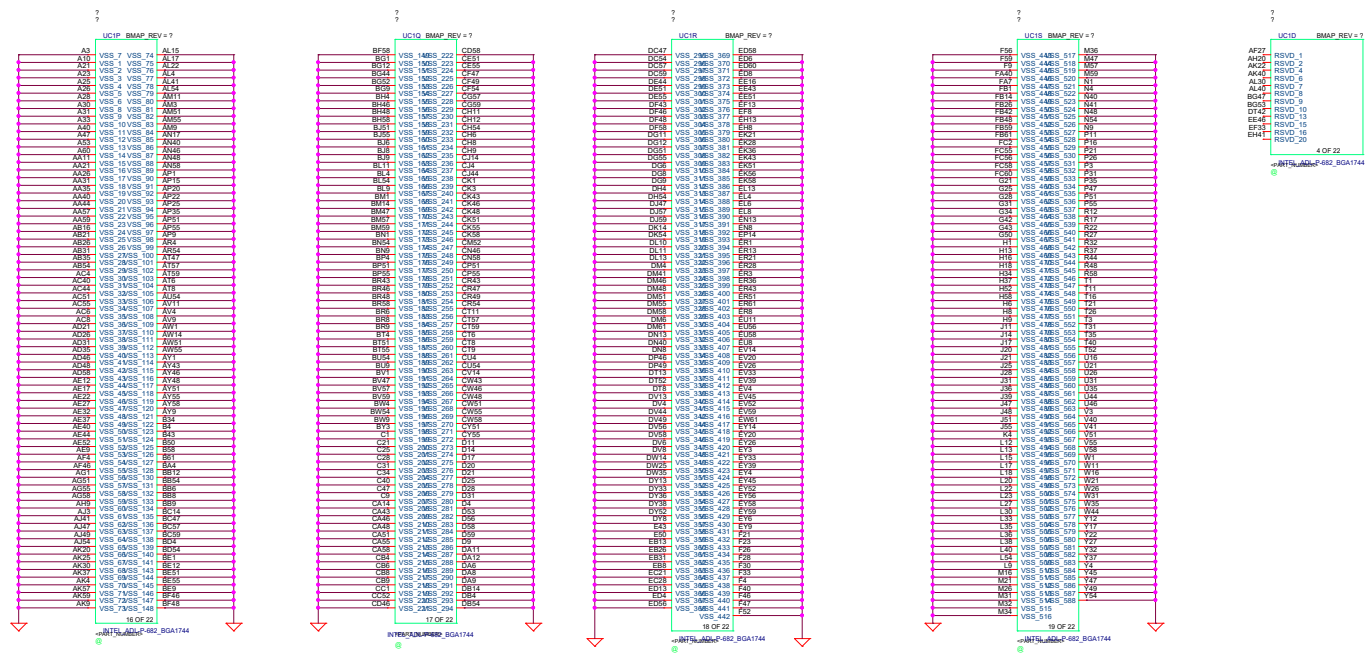


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Note:
RC2524--EC 直接控制enable 时 需要上件
AUX EN delay 控制时, 不要上件;





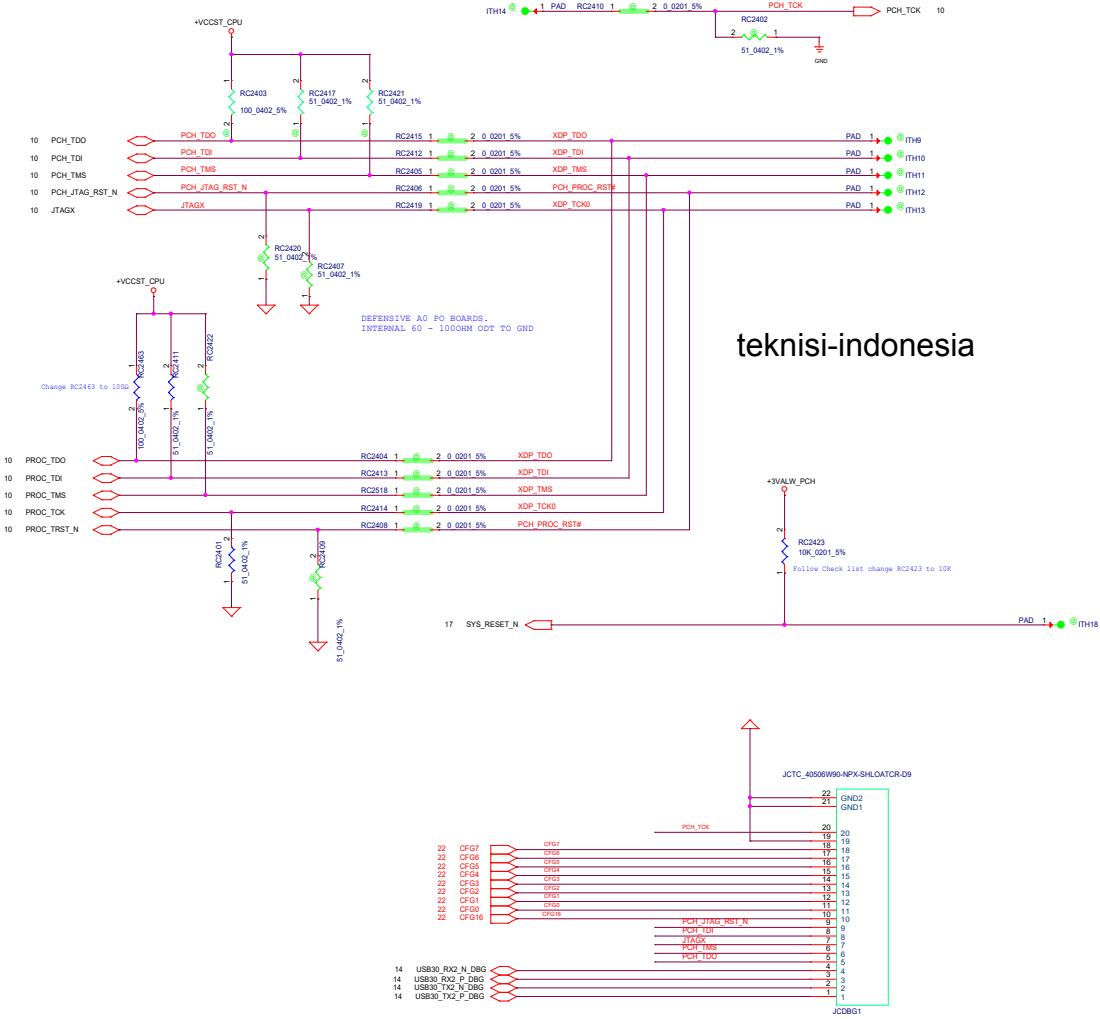
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TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

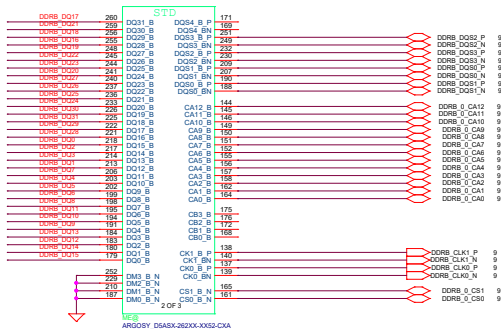


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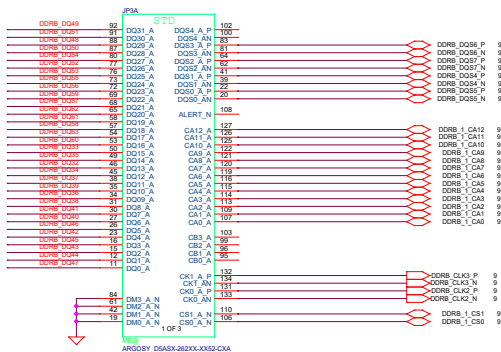
9 DDRB_DQ0_63 DDRB_DQ63_63

JF8B

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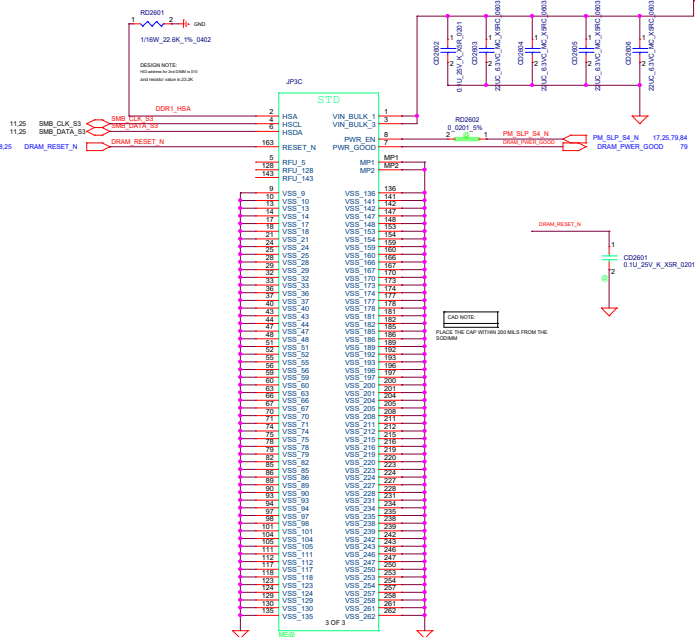


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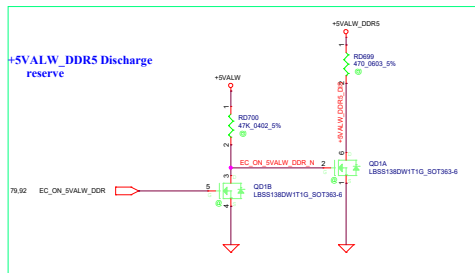
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DESIGN NOTE:
pin 5A1 5A2(1-1) 112

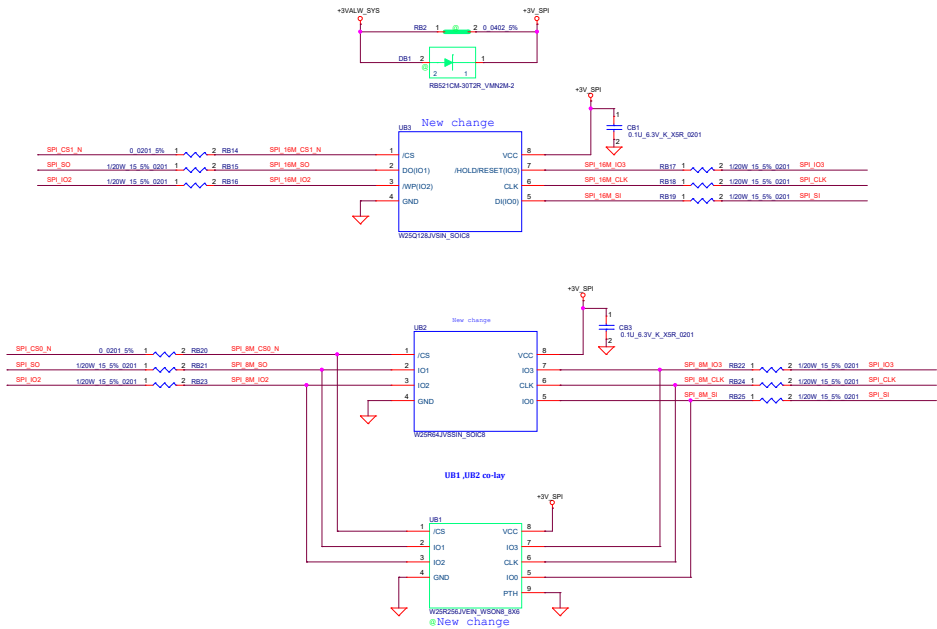
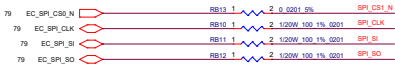
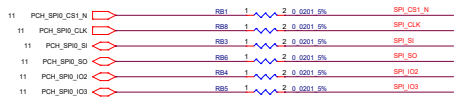


BPAGE DRAWING

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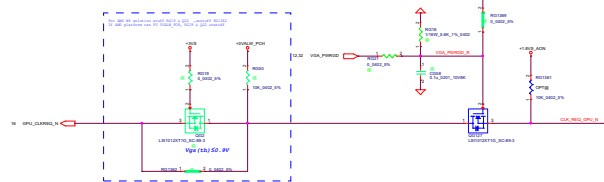
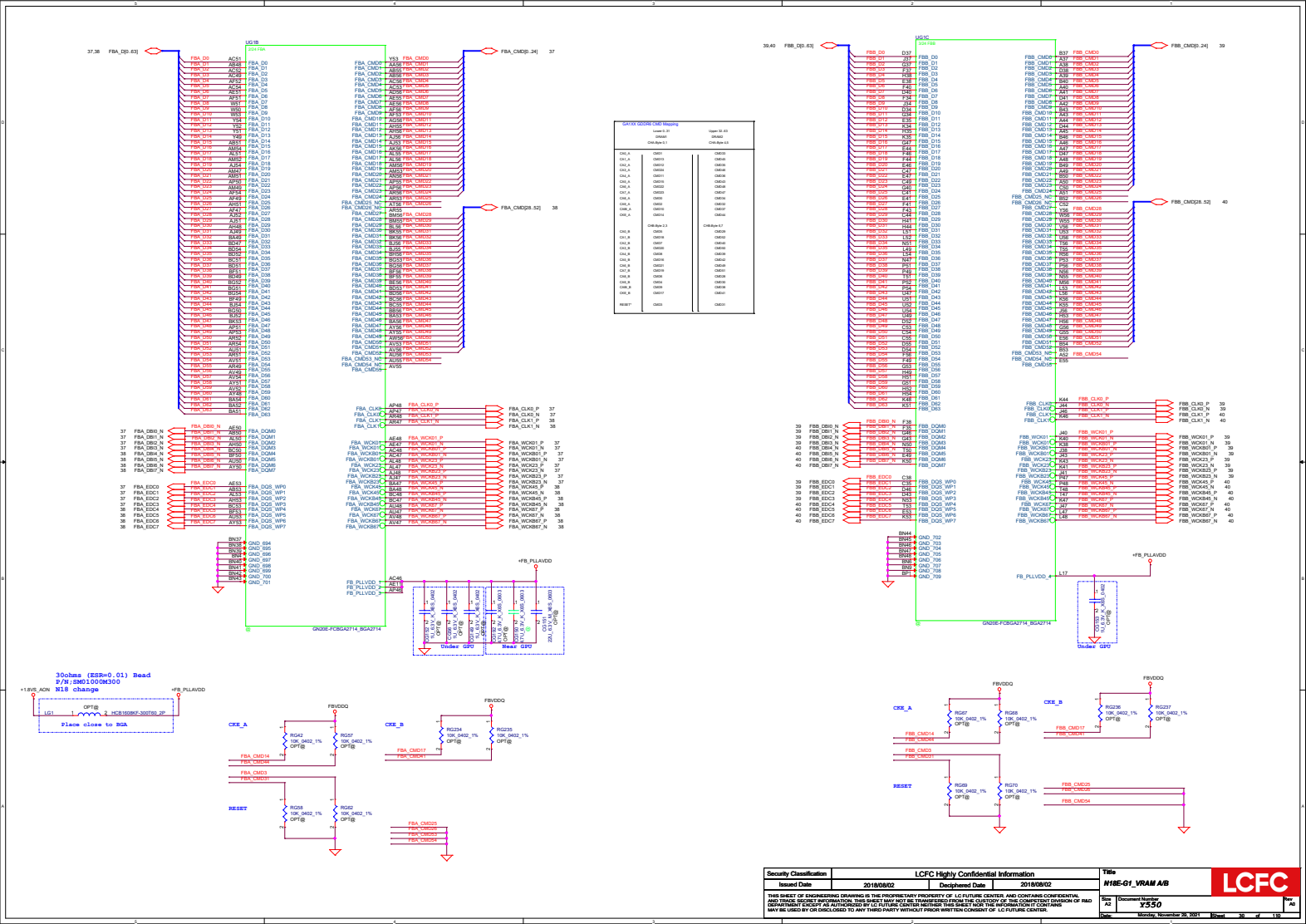
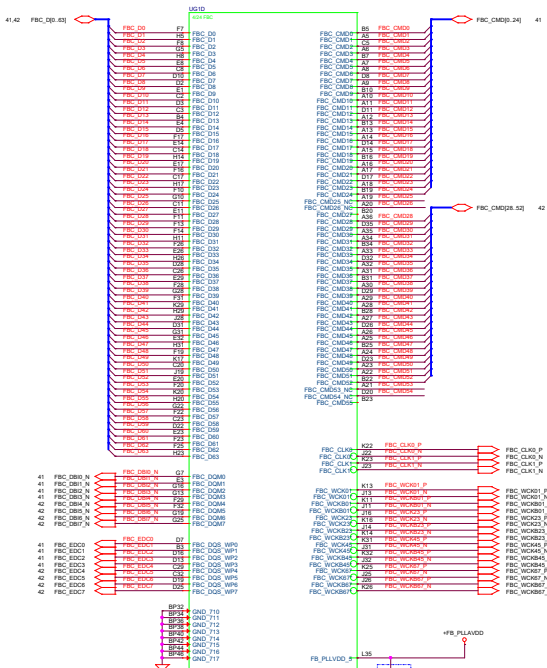
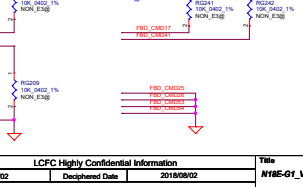
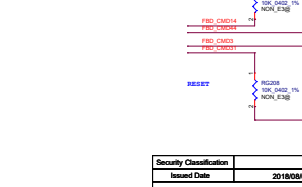
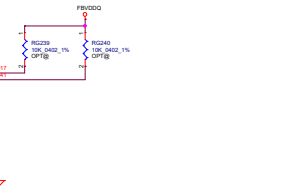
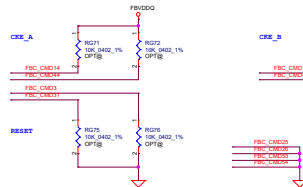
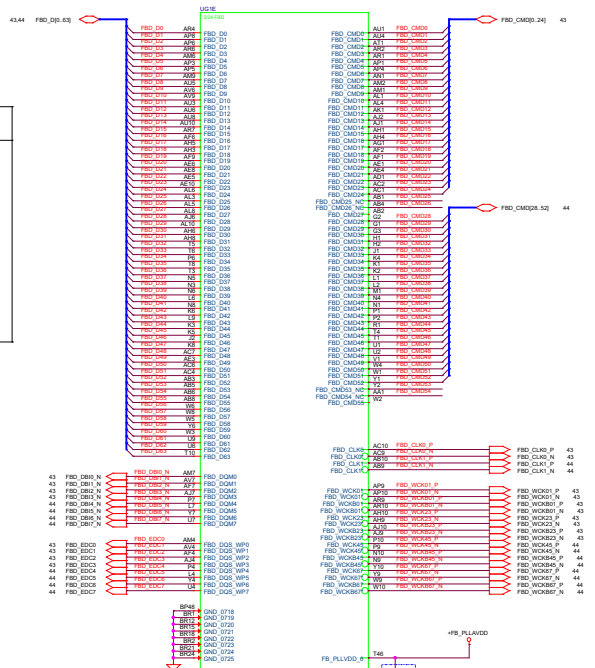


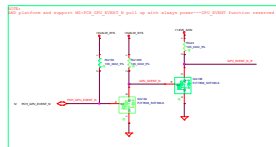
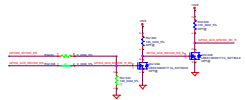
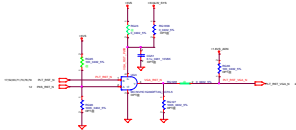
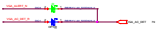
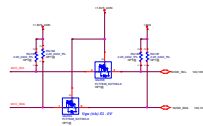
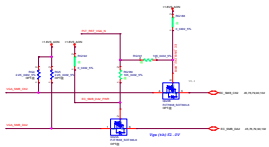
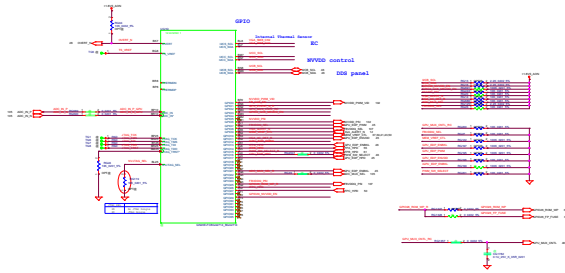
Figure 1: Schematic diagram of the proposed 100-Gbit/s 16-QAM transmitter. The diagram shows a 100-GHz CW laser input, a 100-GHz optical isolator, and a 100-GHz optical circulator. The signal is split into two paths: a main path through a 100-GHz optical isolator and a 100-GHz optical circulator, and a feedback path through a 100-GHz optical isolator and a 100-GHz optical circulator. The main path includes a 100-GHz optical isolator, a 100-GHz optical circulator, and a 100-GHz optical isolator. The feedback path includes a 100-GHz optical isolator, a 100-GHz optical circulator, and a 100-GHz optical isolator. The output is a 100-Gbit/s 16-QAM signal.



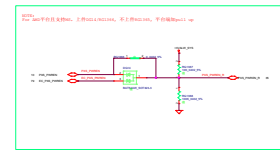
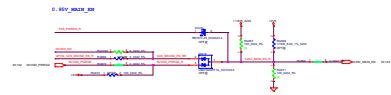
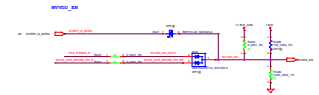


Channel	Controller	Channel	Controller
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FBD_01	FBD_CONTROLLER_01	FBD_09	FBD_CONTROLLER_09
FBD_02	FBD_CONTROLLER_02	FBD_10	FBD_CONTROLLER_10
FBD_03	FBD_CONTROLLER_03	FBD_11	FBD_CONTROLLER_11
FBD_04	FBD_CONTROLLER_04		
FBD_05	FBD_CONTROLLER_05		
FBD_06	FBD_CONTROLLER_06		
FBD_07	FBD_CONTROLLER_07		
FBD_08	FBD_CONTROLLER_08		
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FBD_10	FBD_CONTROLLER_10		
FBD_11	FBD_CONTROLLER_11		

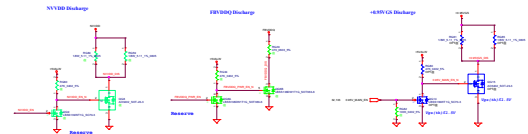


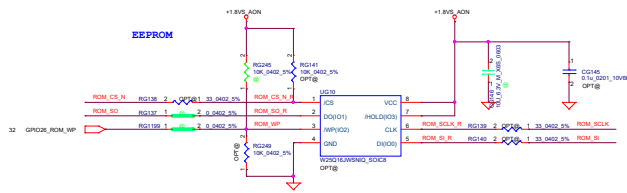
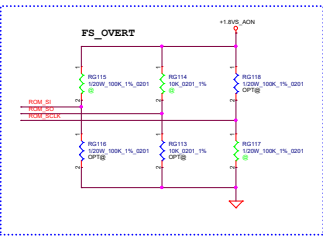
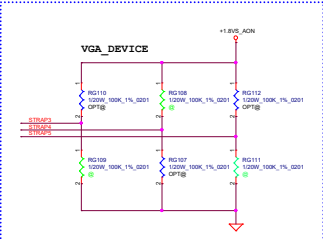
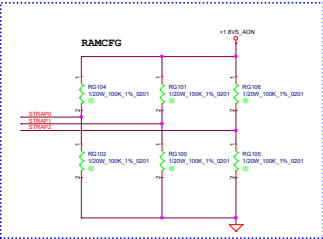
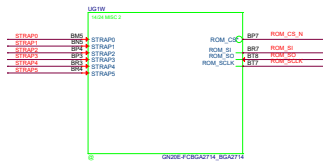


Power on/off sequence



Discharge





GPU VRAM	FB Memory (GDDR6)	RAMCFG[2:0]	STRAP0	STRAP1	STRAP2
GN20x-E7	Samsung 8Gb	K42803258C-BC14	0 (0x0000)	L	L
	Samsung 16Gb	K42AF3258M-BC 14	9 (0x0009)	L	M

GPU VRAM	FB Memory (GDDR6)	RAMCFG[2:0]	STRAP0	STRAP1	STRAP2
GN20x-E5	Samsung 8Gb	K42803258C-BC14	0 (0x0000)	L	L
GN20x-E3	Microon 8Gb	MT61K250K32JE-14: A	1 (0x0001)	H	L
	Bynlix 8Gb	H56CB824L18-S2C	2 (0x0002)	L	R

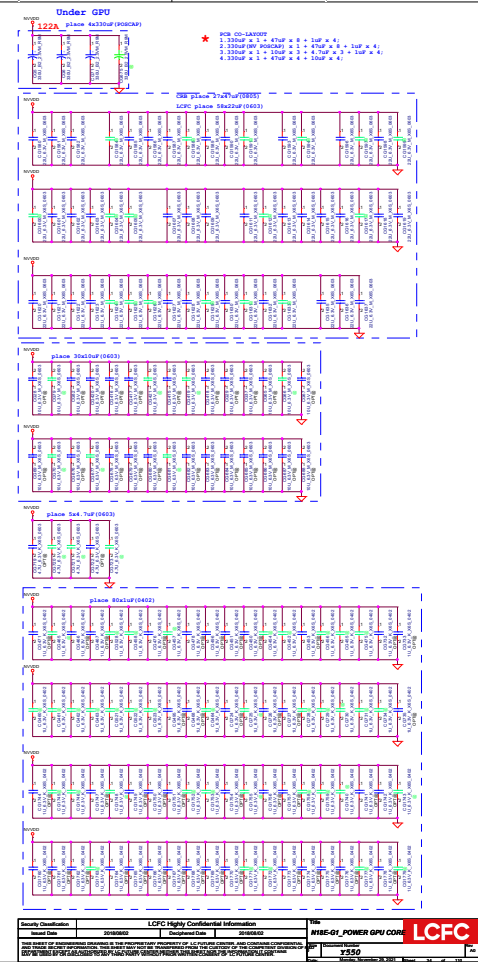
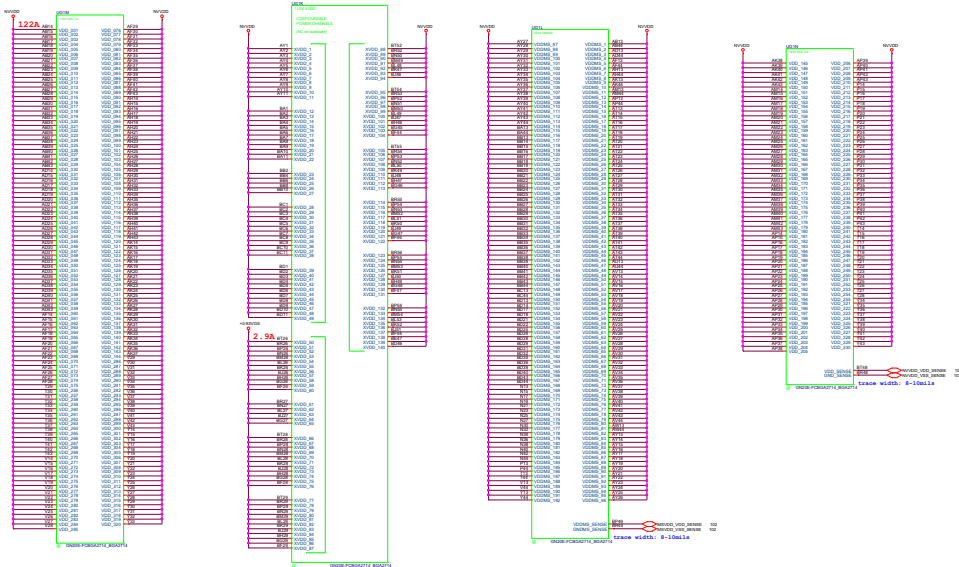
GPU VRAM	FB Memory (GDDR6)	RAMCFG[2:0]	STRAP0	STRAP1	STRAP2
	Bynlix 16Gb	H56G42A84DX014	8 (0x0008)	M	L
GN20x-E6	Samsung 16Gb	K42AF3258M-BC16	6 (0x0006)	L	R
	Bynlix 8Gb	H56G32C94DX005	5 (0x0005)	H	L

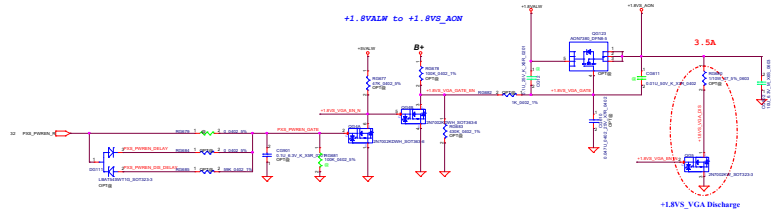
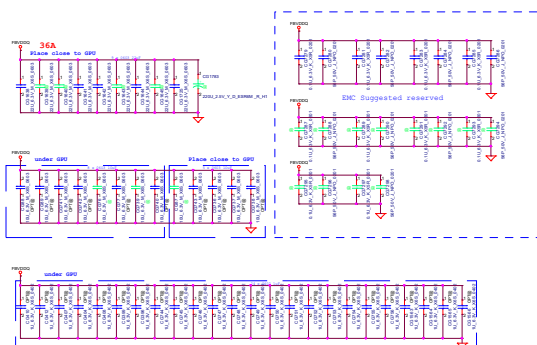
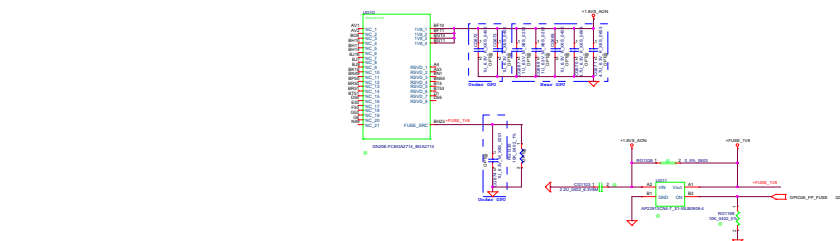
VGA_DEVICE E3E5E7						
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
H	L	H	0	1	0	1

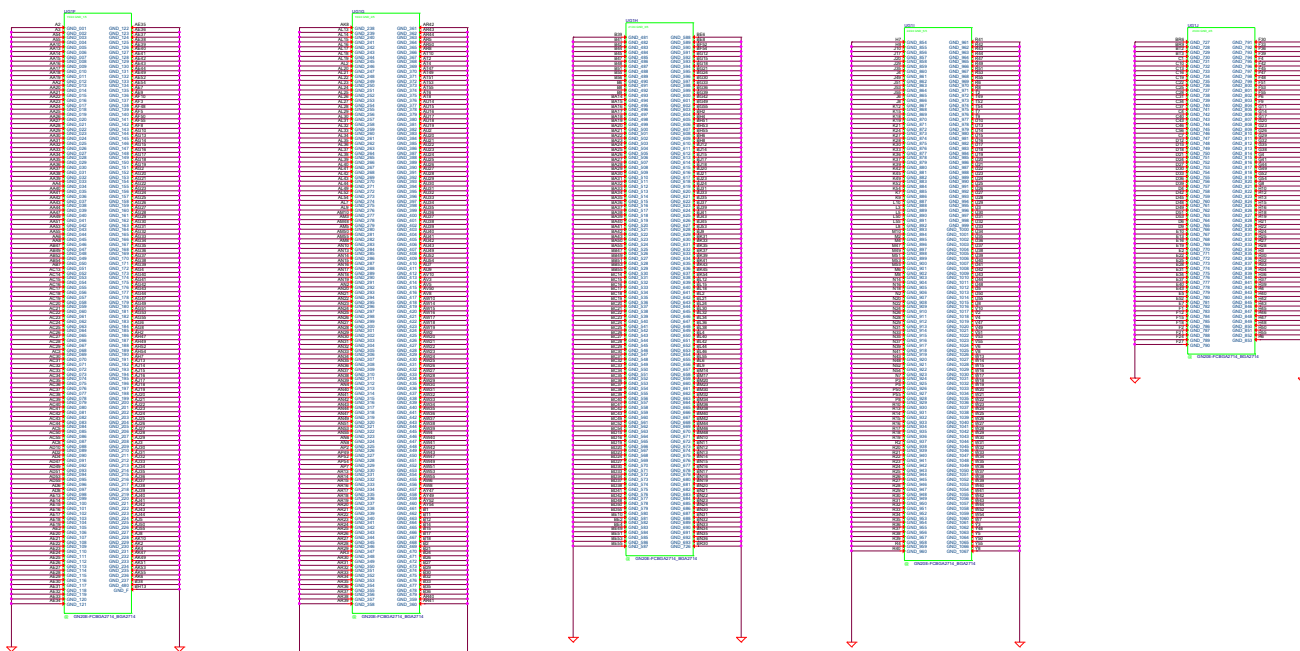
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

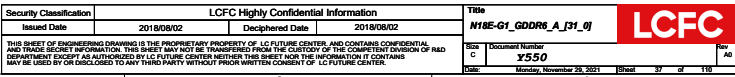
GPU	ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT
GN20x	L	L	H	ENABLE

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Issued Date	20180802	Disphelred Date	20180802	NIIE-01 JWSH IF
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Doc No	Y550	Doc Number	Y550	Rev
Doc	Monday, November 26, 2018	Doc	33	110





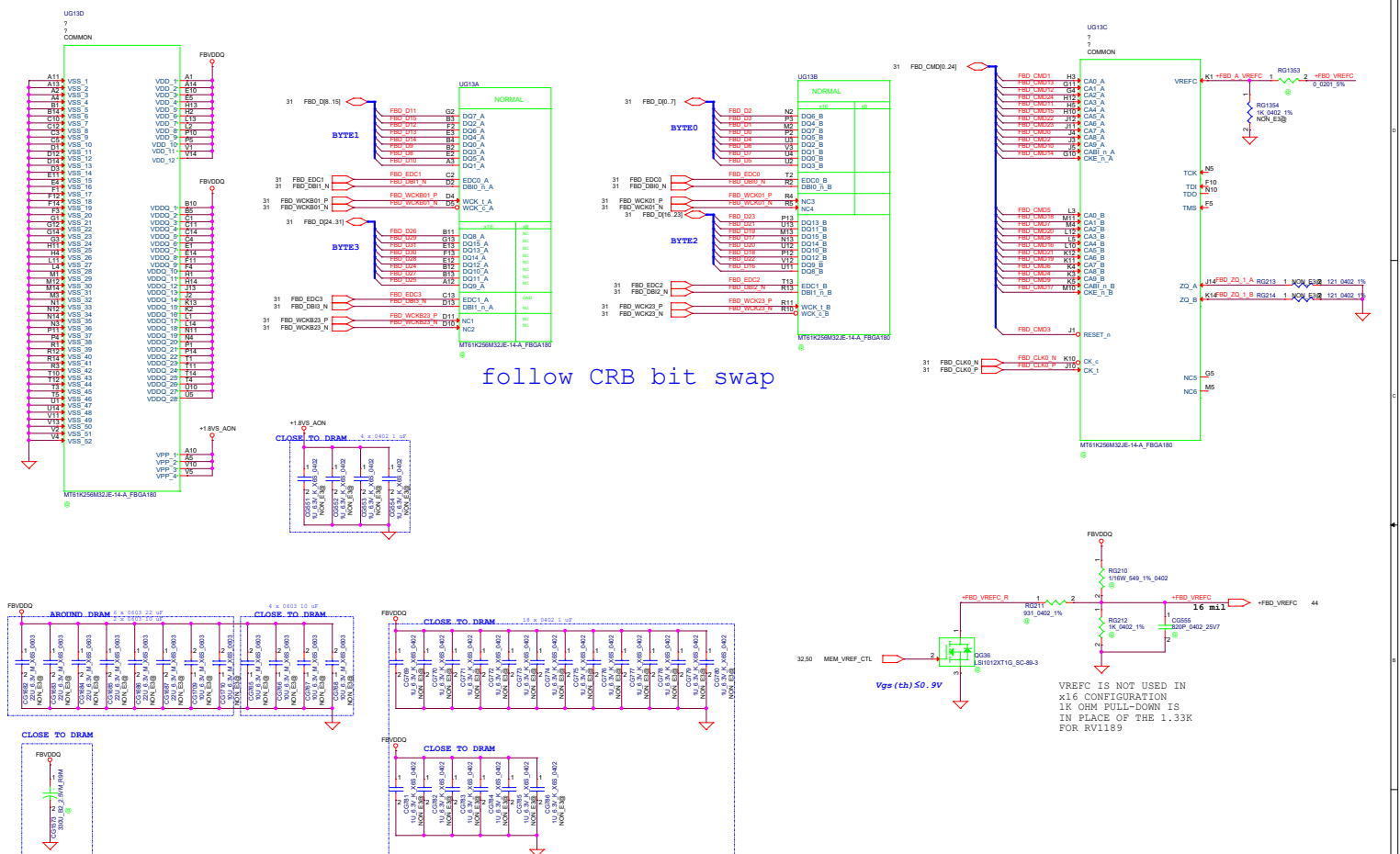




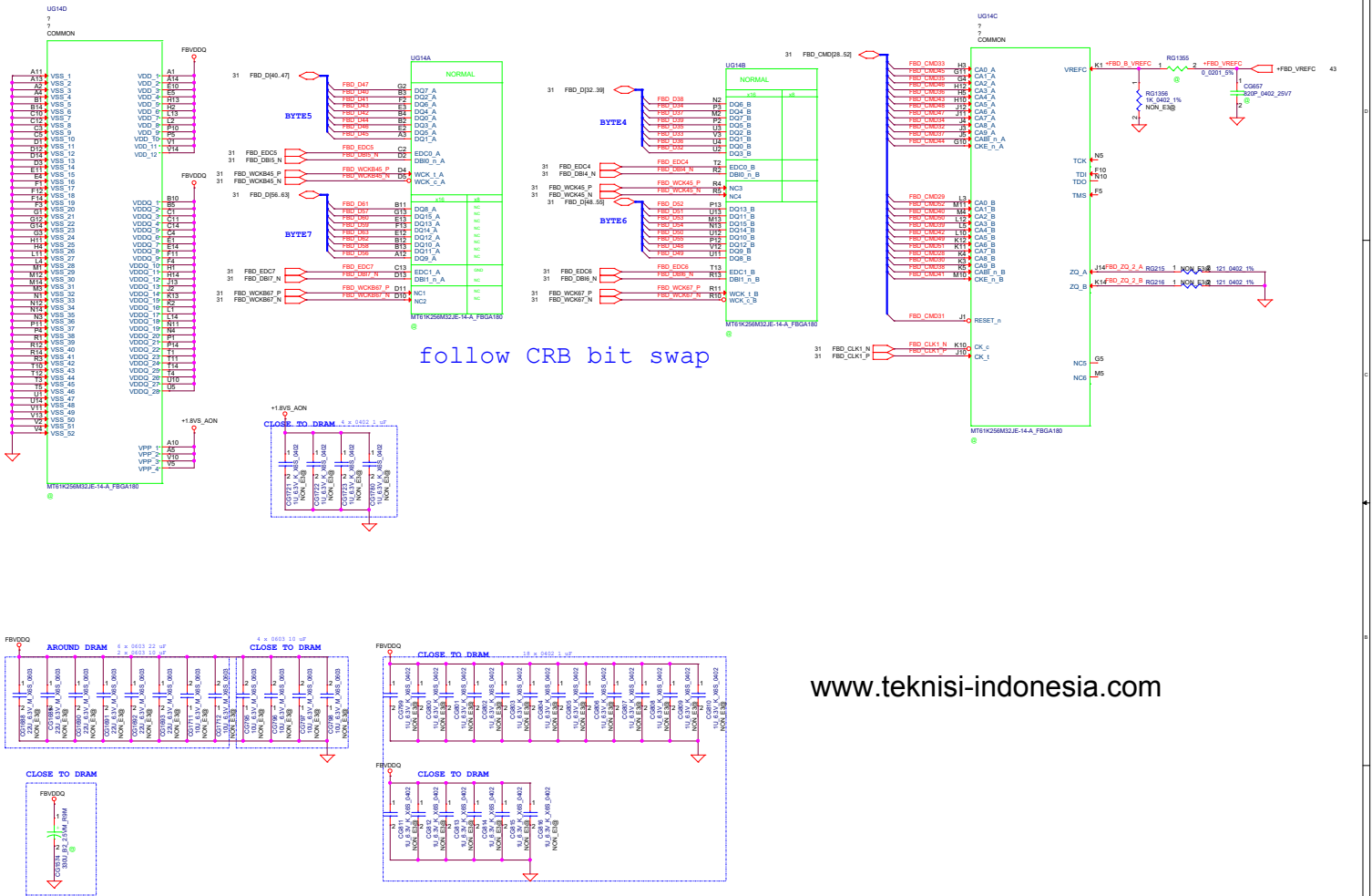
follow CRB bit swap

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				Date Monday, November 26, 2021	Page 38 of 116



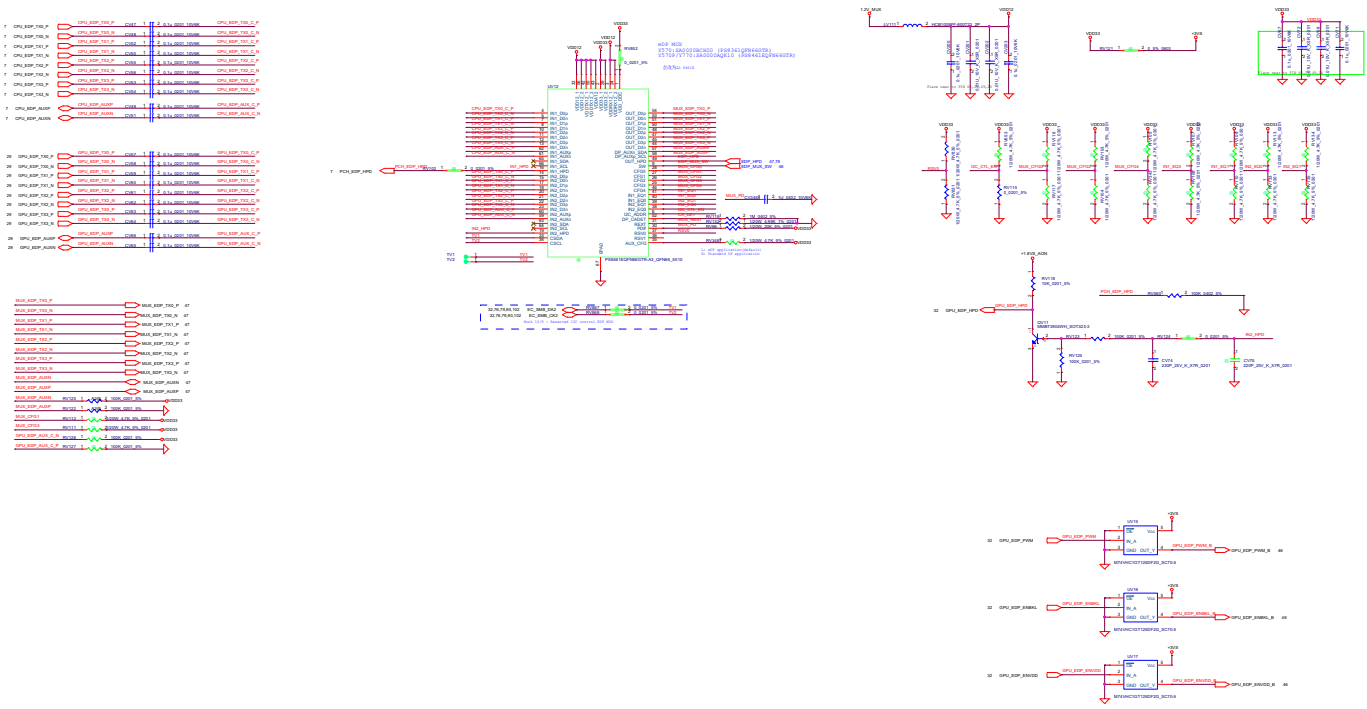
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				Rev	A0
				Date	Monday, November 25, 2021
				Page	43 of 116

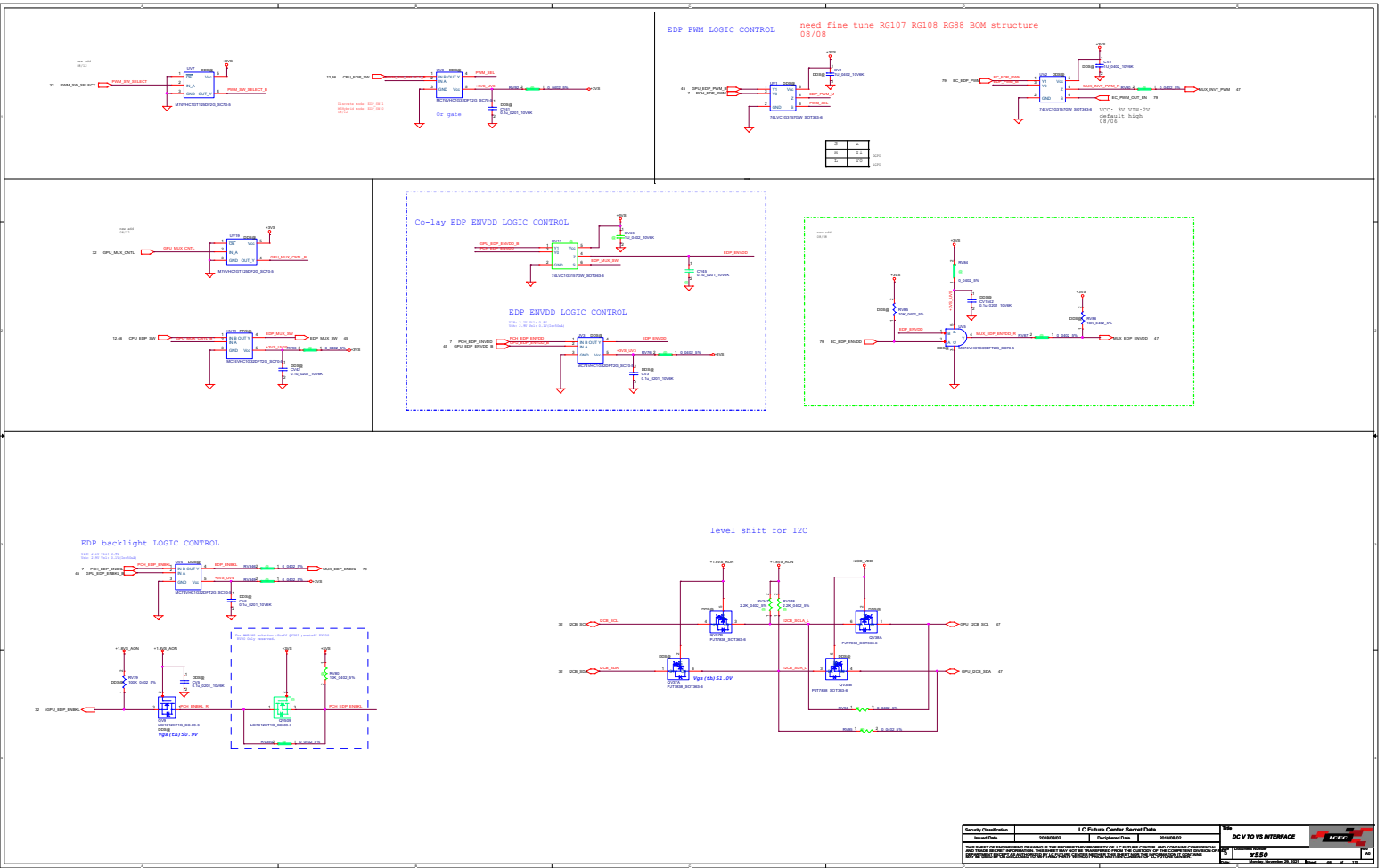


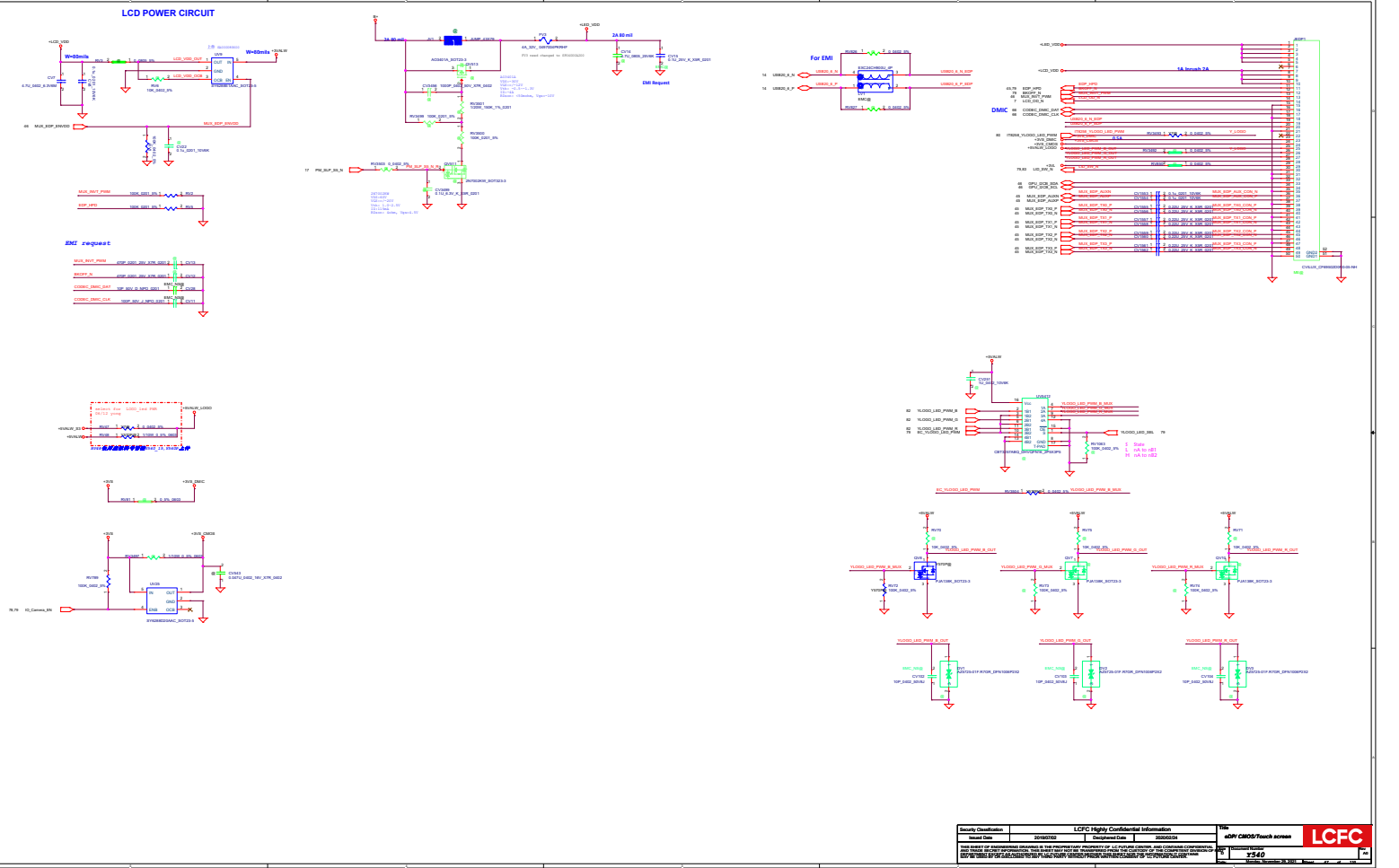
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				44	116

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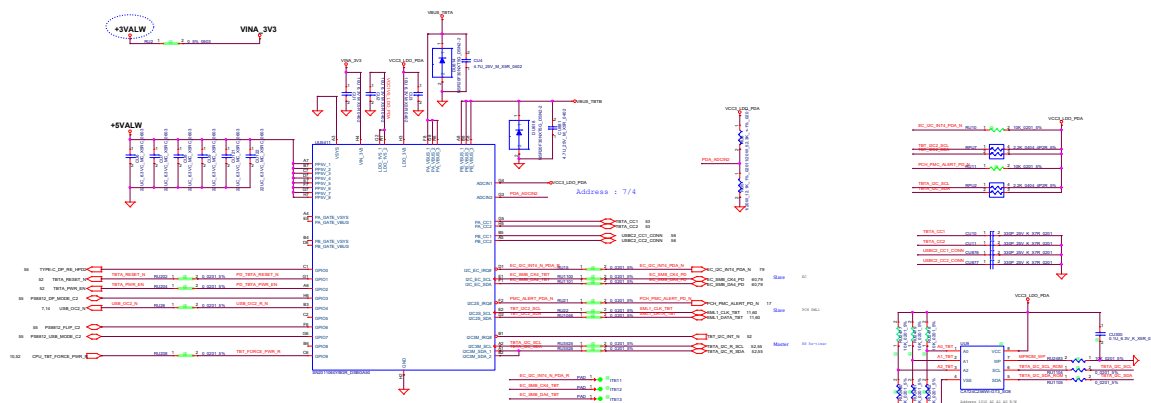




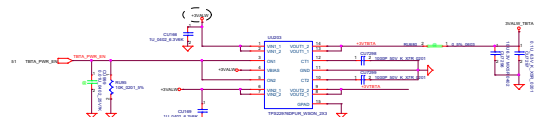
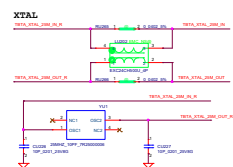
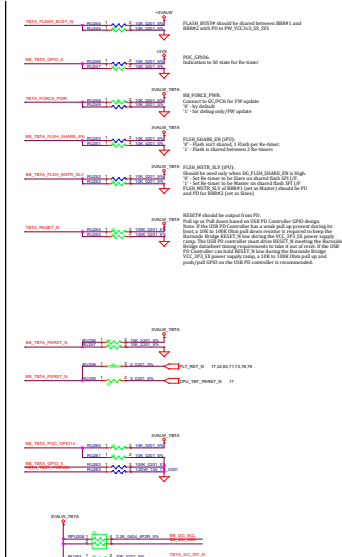
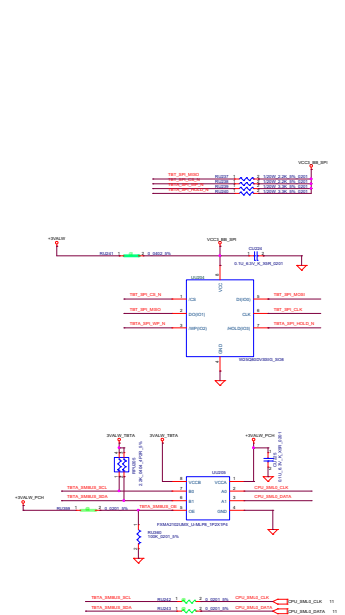
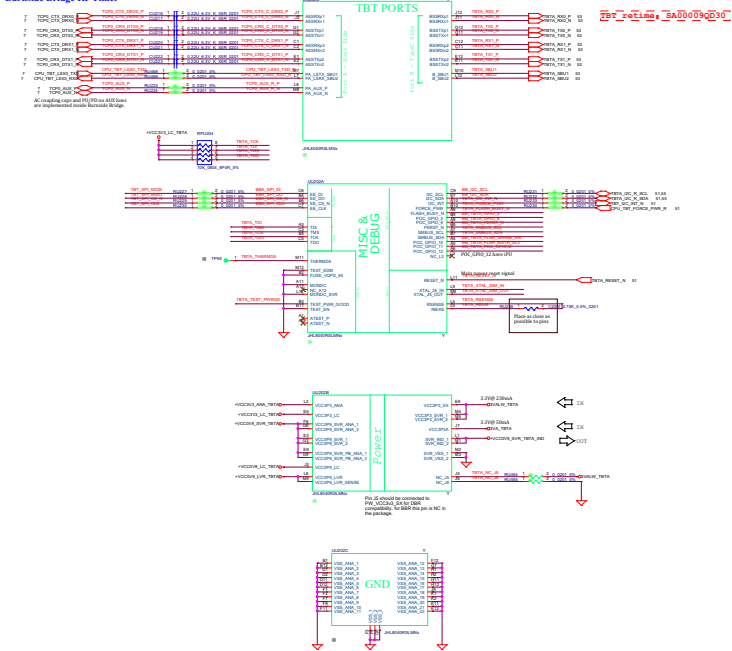


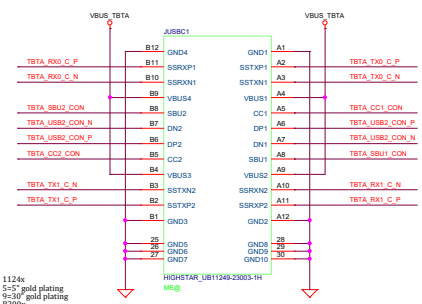
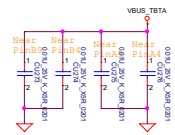
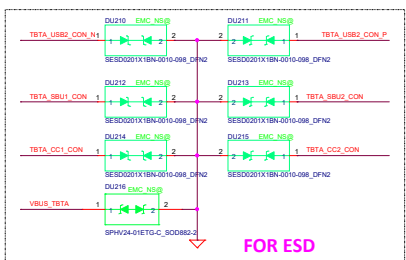
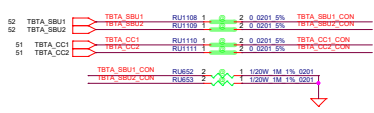
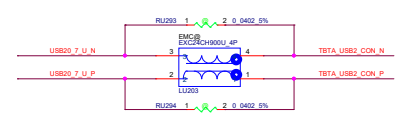
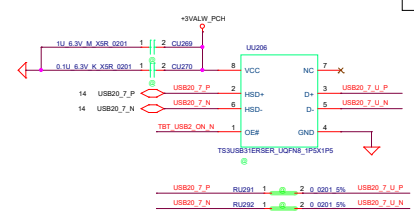
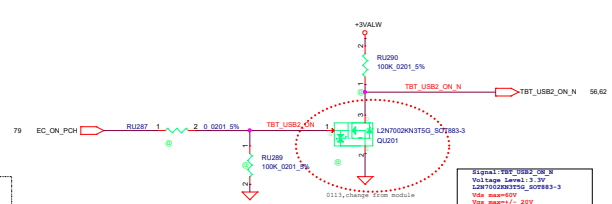
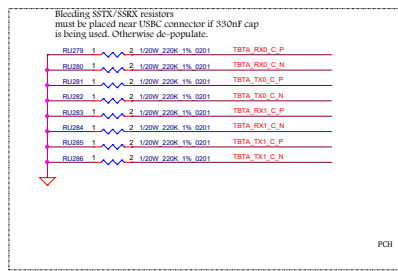
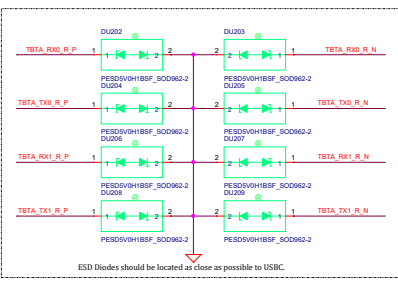
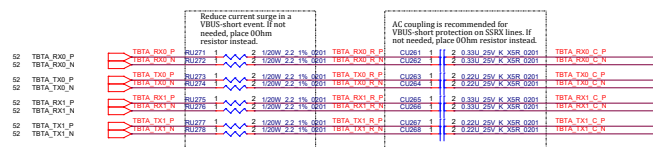
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Size A	Document Number <Doc>		Date: Monday, November 29, 2021
Sheet 49		of 110	


TBT portA/rear side

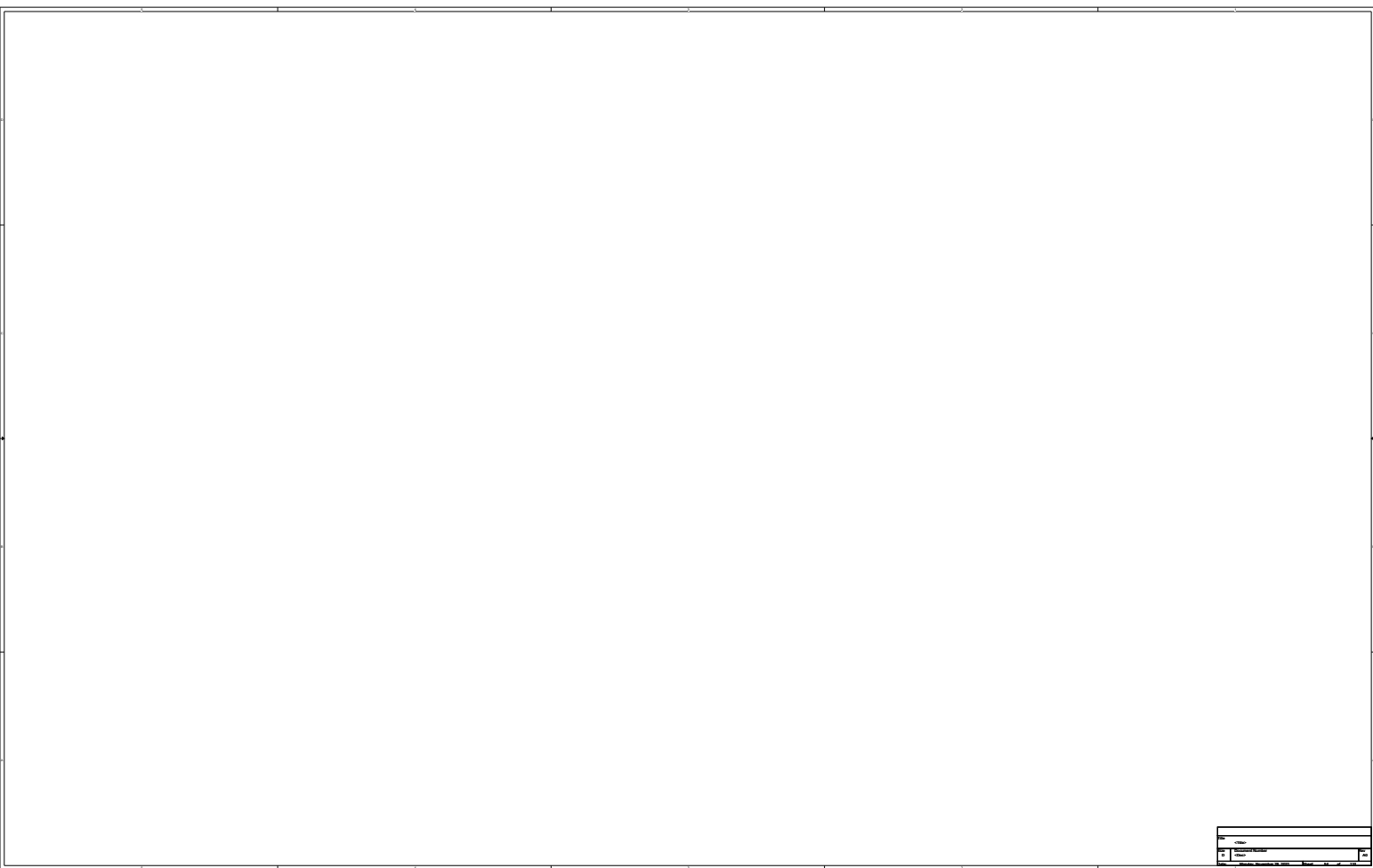


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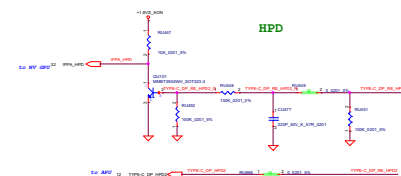
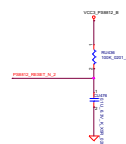
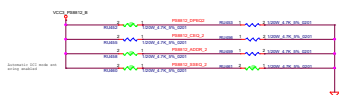
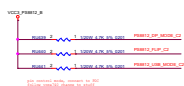
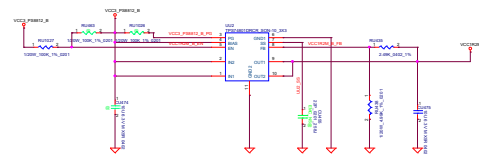
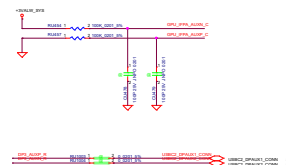
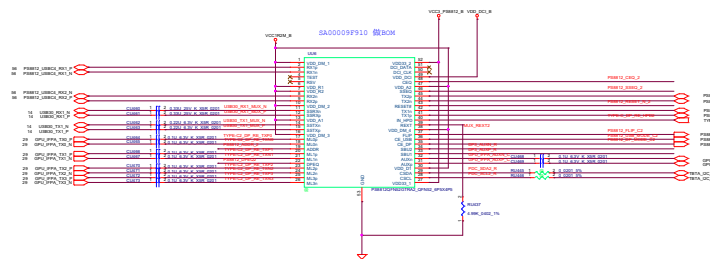
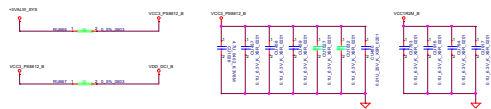


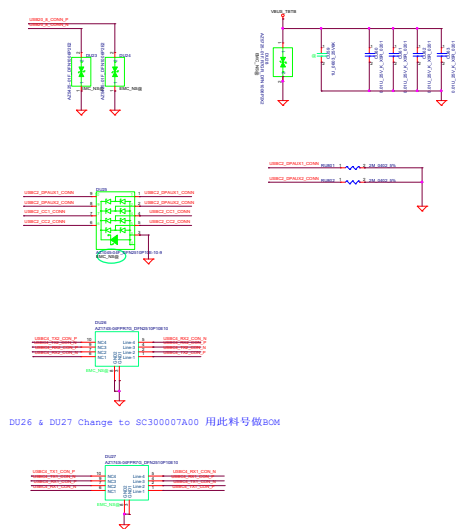


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Date		
Page		
Author		
Title		
Subject		
Keywords		
Abstract		
References		
Notes		
Comments		
Footer		

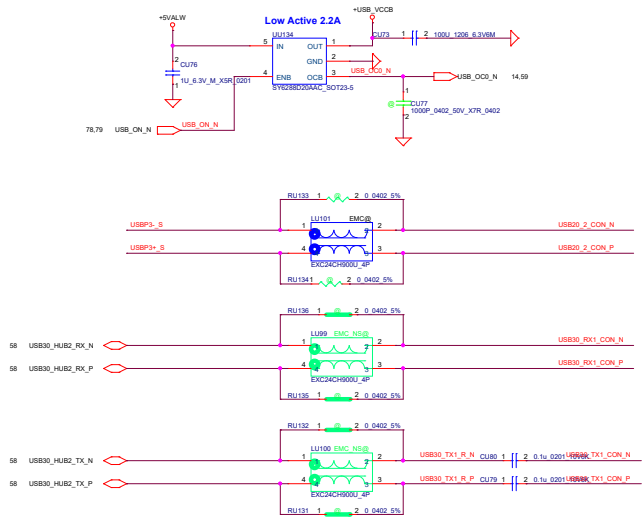




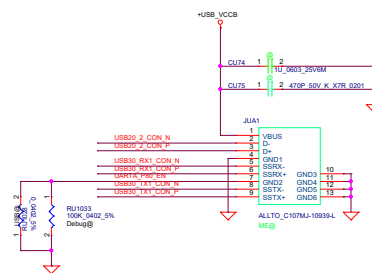
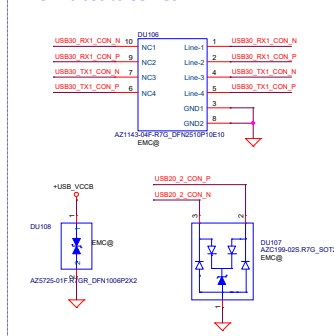
DU26 & DU27 Change to SC300007A00 用此料号做BOM

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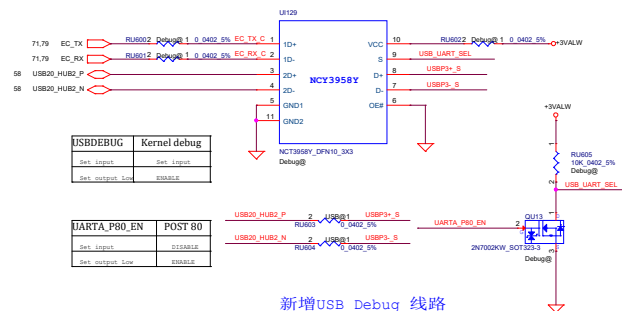
USB3.1 PORT x2



EMC close to USB Conn



For USB Debug Function




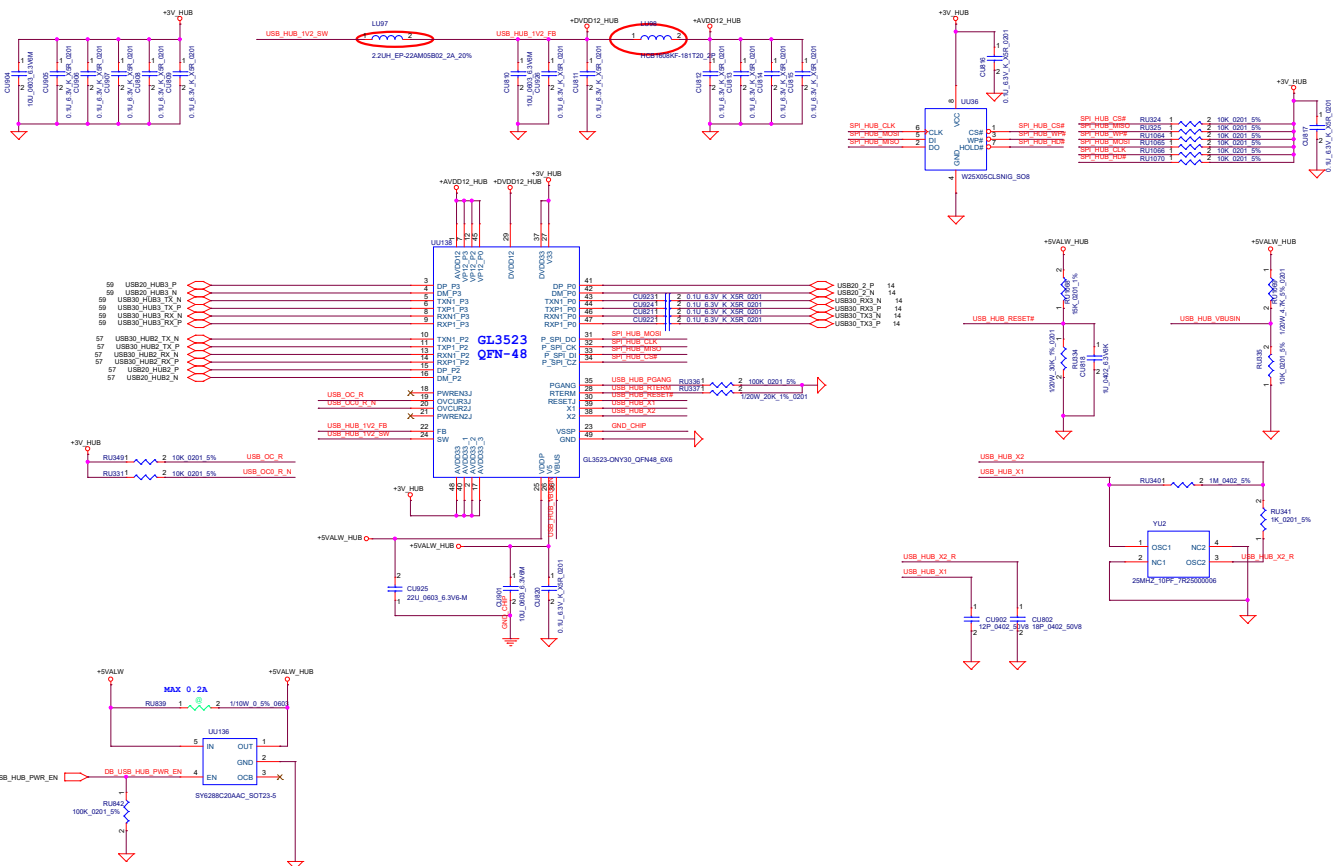
USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

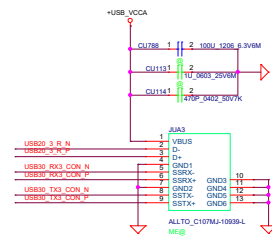
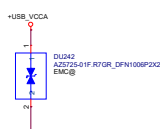
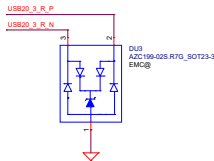
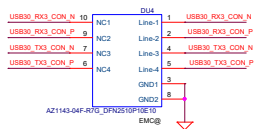
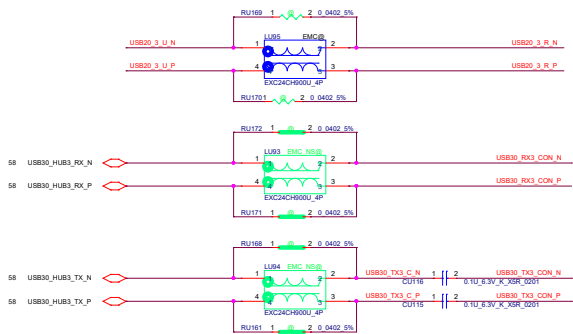
OE#	S	FUNCTION
H	X	DISABLE
L	L	D(s/-) to 1D(s/-)
L	H	D(s/+) to 2D(s/+)

新增USB Debug 线路

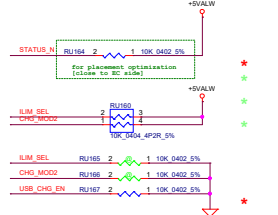
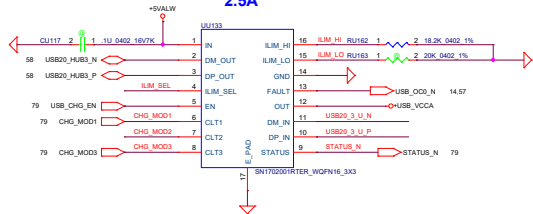
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Date	Monday, November 26, 2021		Sheet	57 of 119



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Rev C		Document Number		Monday, November 25, 2017		Sheet 68 of 118	

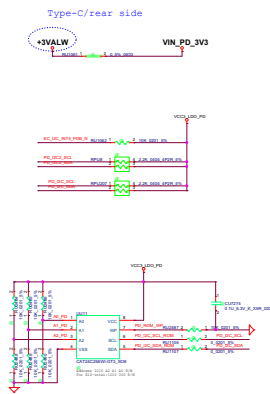
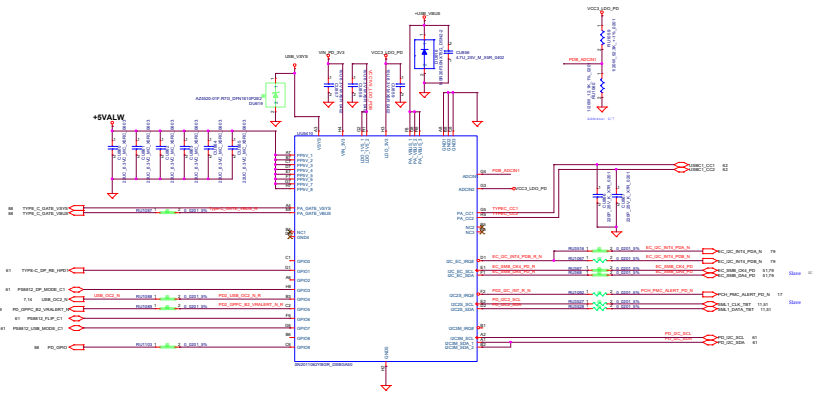


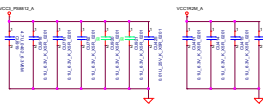
USB charger 2.5A



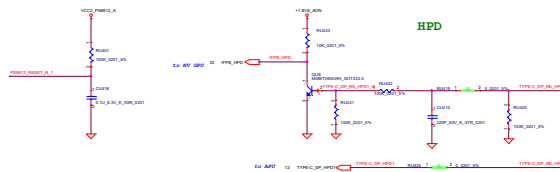
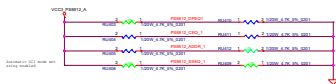
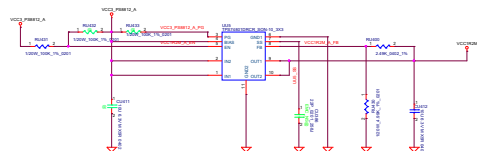
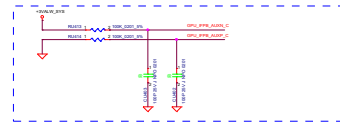
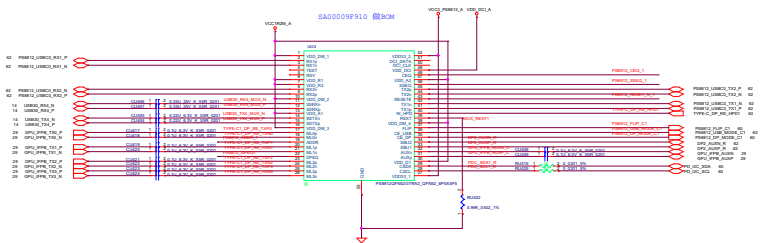
CLT1	CLT2	CLT3	ILM_SEL	MOD
0	0	0	X	DCR Out held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active

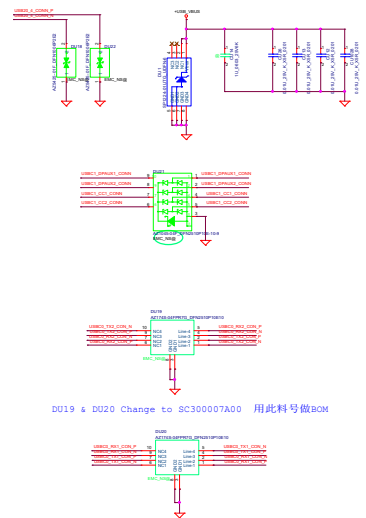
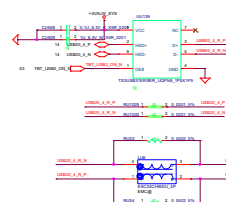
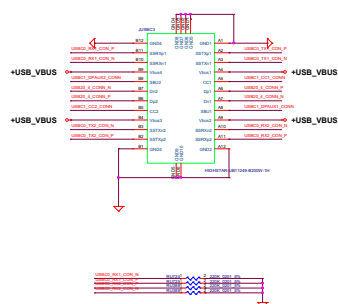
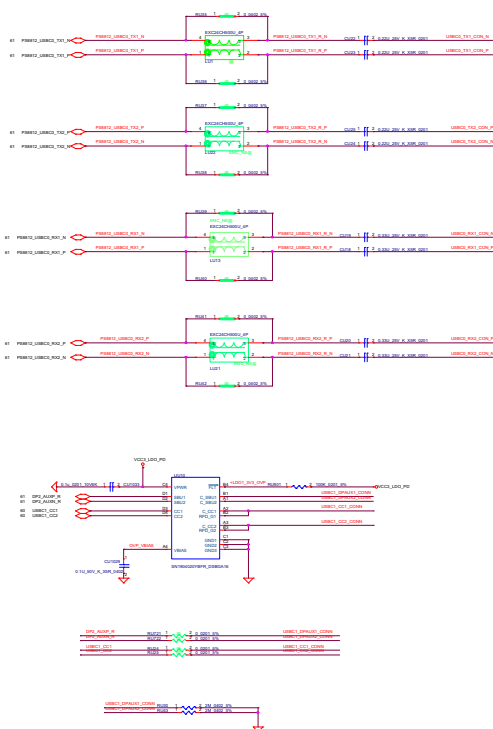
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	USB2.0/USB3.0 PORT (LEFT)	
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Size	Document Number			Rev	
	Y550			A0	
Date	Version			15	
	15			15	





SAD000SF10

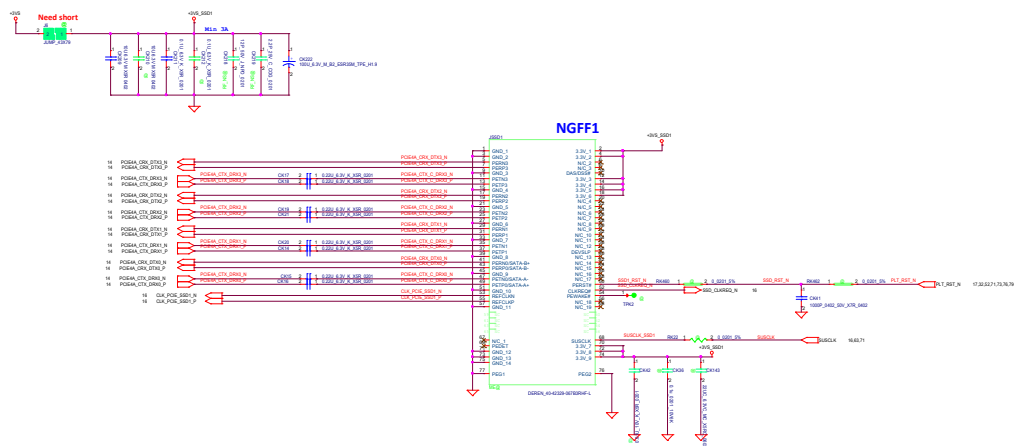




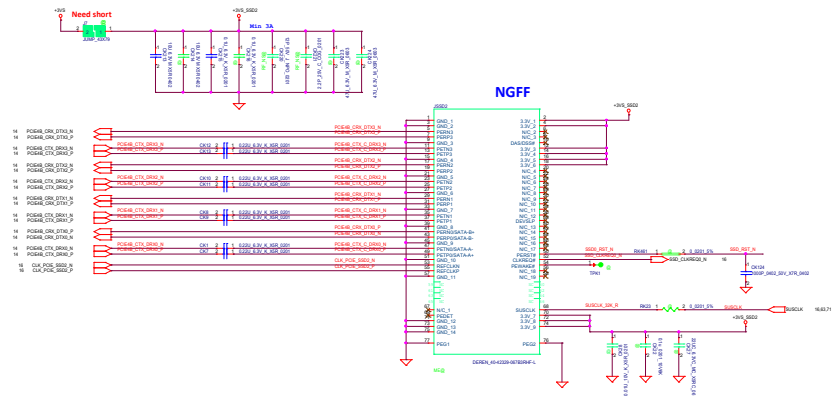
DU19 & DU20 Change to SC300007A00 用此料号做BOM

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M.2 SSD(PCIE GEN4 from CPU)

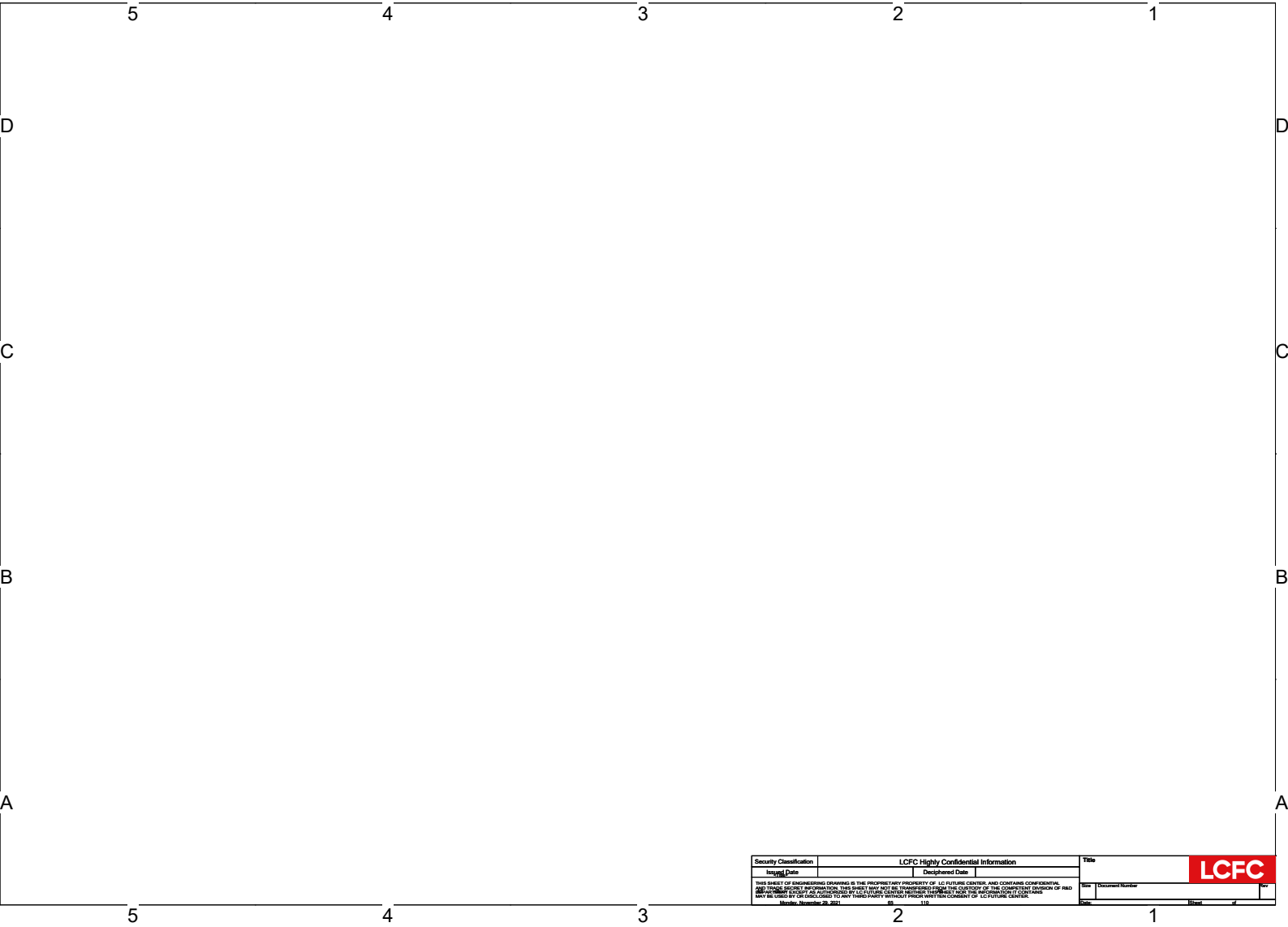


M.2 SSD(SATA/PCIE Gen3 from PCH)

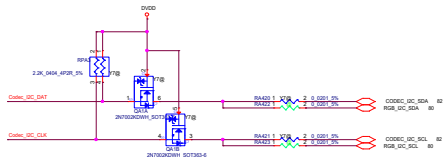
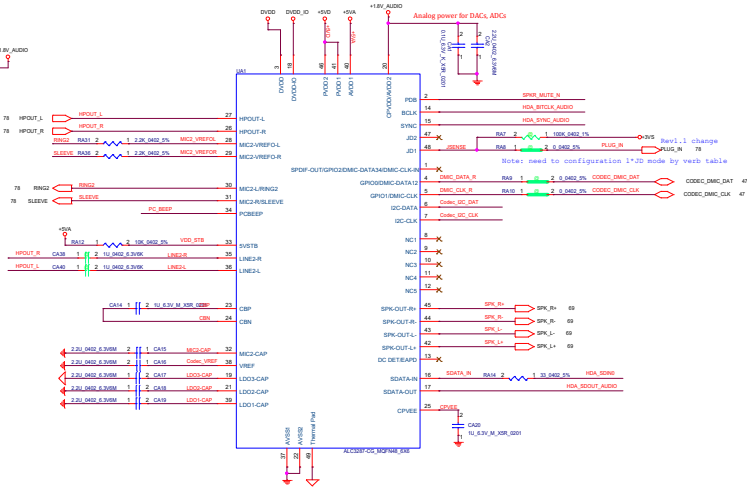
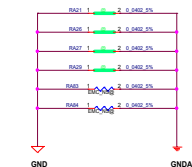
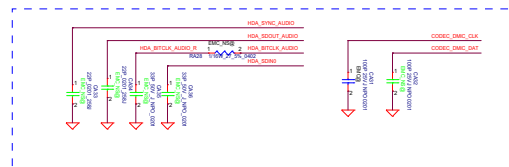
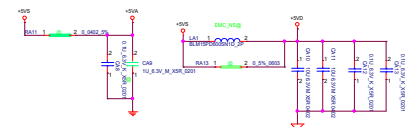
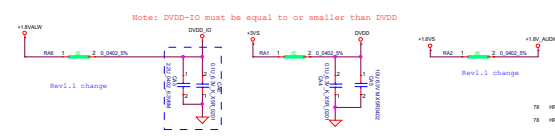


Delete USB3.0 Reapter Remove to DB board

Security Classification	LCFC Highly Confidential Information		Title		<div>LCFC</div>	
Issued Date	2019/07/02	Deciphered Date	2020/02/24	DC V TO VS INTERFACE		
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				C	Y540	A0
				Issue	Monday, November 25, 2021	Sheet 64 of 119



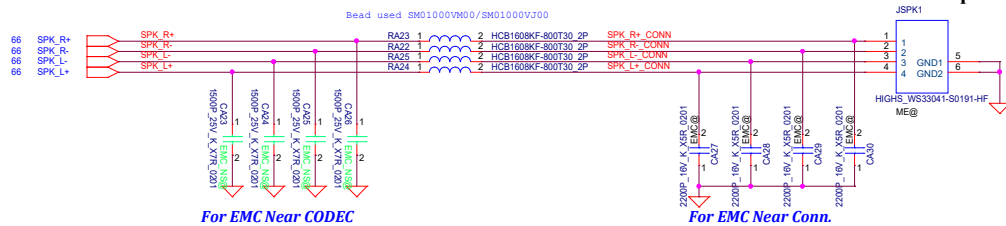
13 HDA_BTCLK_AUDIO
13 HDA_SYNC_AUDIO
13 HDA_SDOUP_AUDIO
13 HDA_SDOIN
13 HDA_SDR0



Security Classification	LCFC Highly Confidential Information		Title	Common Module	LCFC
Issued Date	2012/07/01	Deciphered Date	2014/07/01		
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Rev	C			Document Number	Rev
				Audio Amplifier	Alt
Date				Version	2014-07-01
Sheet				67	of 110

Speaker

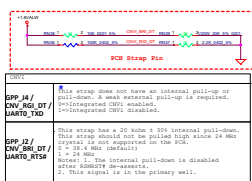
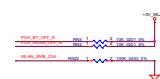
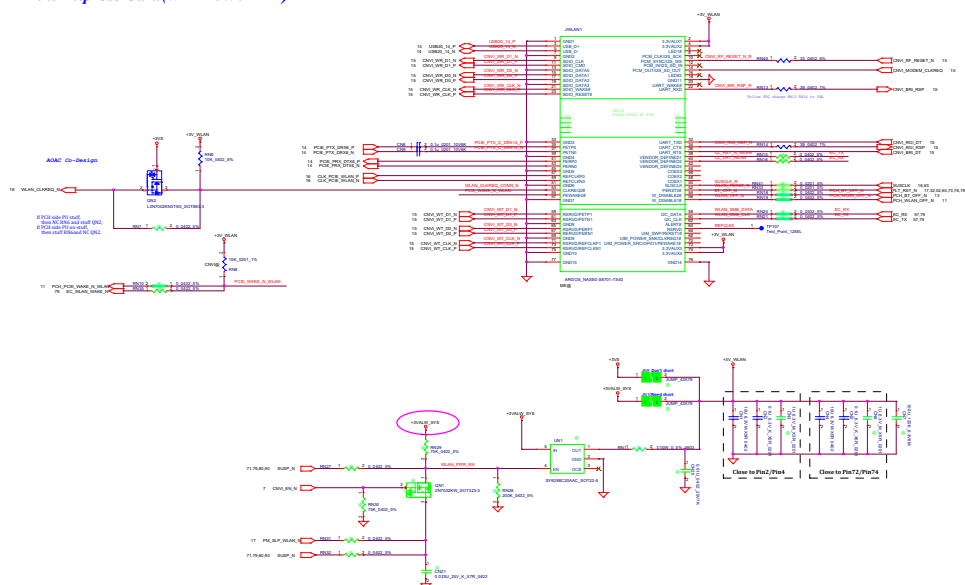
Speaker




Security Classification		LCFC Highly Confidential Information		Title S540-TGL		LCFC
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Size B	Document Number Audio SPK/Jack	
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Date: Monday, November 26, 2021						Sheet 69 of 110

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Issued Date	2019/07/02	Deciphered Date	2020/02/24		
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				C	Y540
				Date	Monday, November 25, 2021
				Sheet	70 of 115

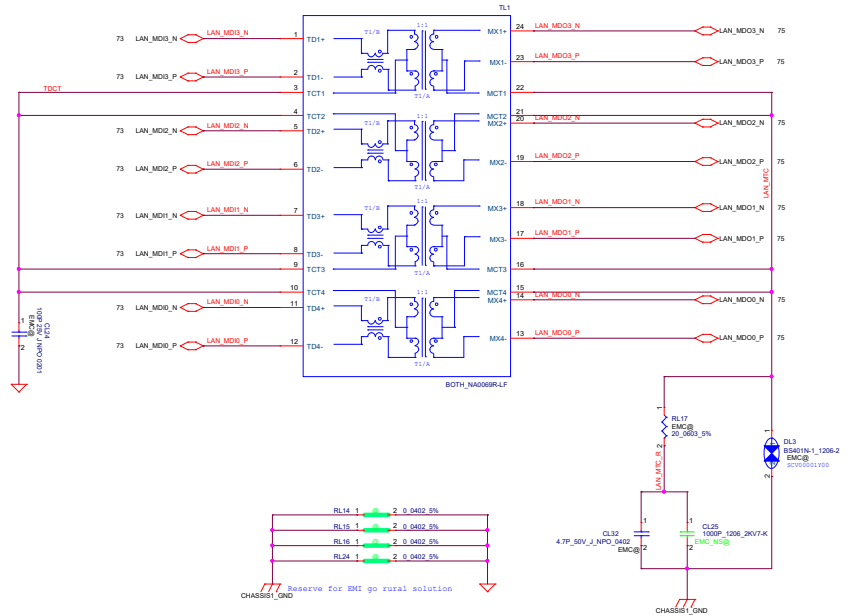
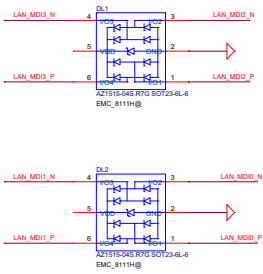
Mini-Express Card(WLAN/WiMAX)



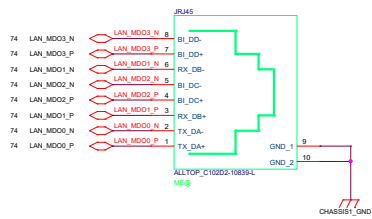
Security Classification		LC Future Center Secret Data		Title	
Issued Date		Declassified Date		CNVI	
20180802		20180802			
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				Classified Xr60	
				Date: November 20, 2020	Page: 2 / 2

Security Classification		LC Future Center Secret Data		Title		
Issued Date	2019/11/06	Deciphered Date	2019/11/05	Yx60-Reserved		
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Size		Document Number		Reserved Date: Monday, November 29, 2021 Sheet 72 of 110		

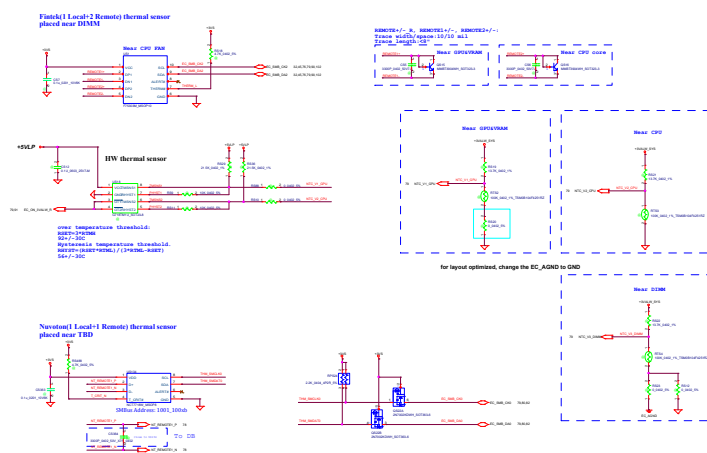
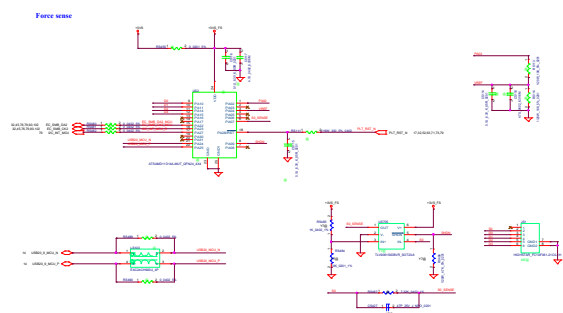
DL1/DL2
1'S PN:SC300005900
Place Close to TL1



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Issued Date	2019/07/02	Deciphered Date	2020/02/24	DC V to VS INTERFACE	
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				Y540	Rev A0
				Issue	1
				Sheet	74 of 115

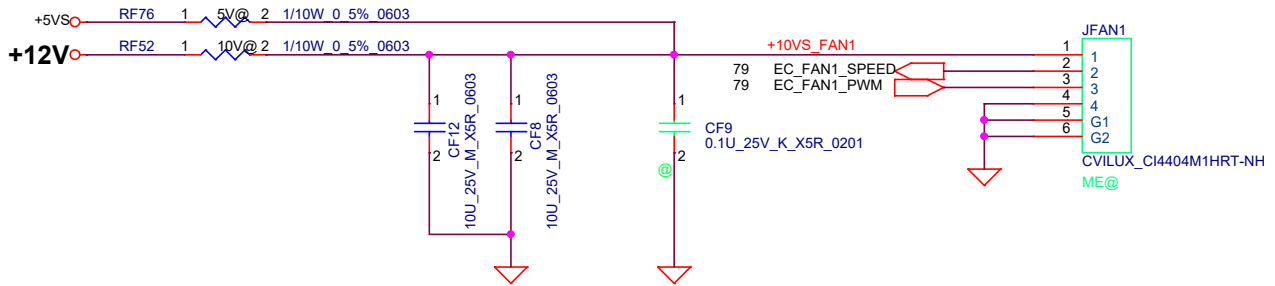


Security Classification		LCFC Highly Confidential Information		Title	
Issued Date		Deciphered Date		LAN_Transformer	
2019/07/02		2020/02/24		LCFC	
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				Size	Document Number
				5	Y540
				Date	Monday, November 18, 2021
				Sheet	75 of 110



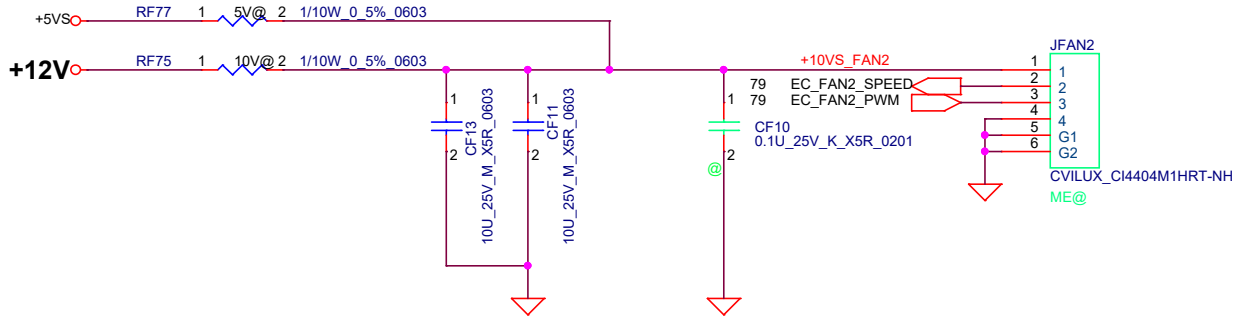
Remove TOF sensor

FAN Conn Right



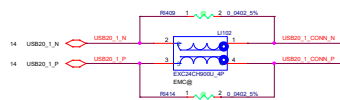
22U 电容换成两颗10U 0603 电容 TOP 和BOT各放一颗增加5VS 供电

FAN Conn LEFT

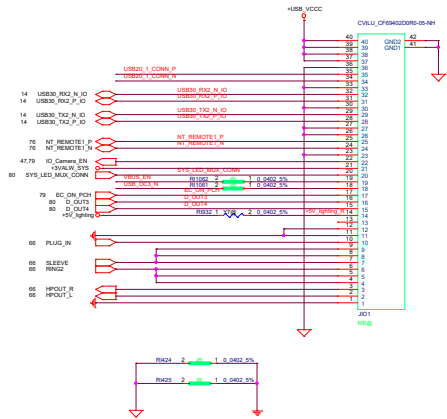
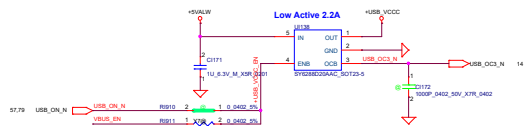


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Issued Date	2019/07/02	Deciphered Date	2020/02/24		Thermal sensor/FAN CONN									
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						A	Y540	A0						
						Date: Monday, November 29, 2021					Sheet	77	of	110
											2	1		

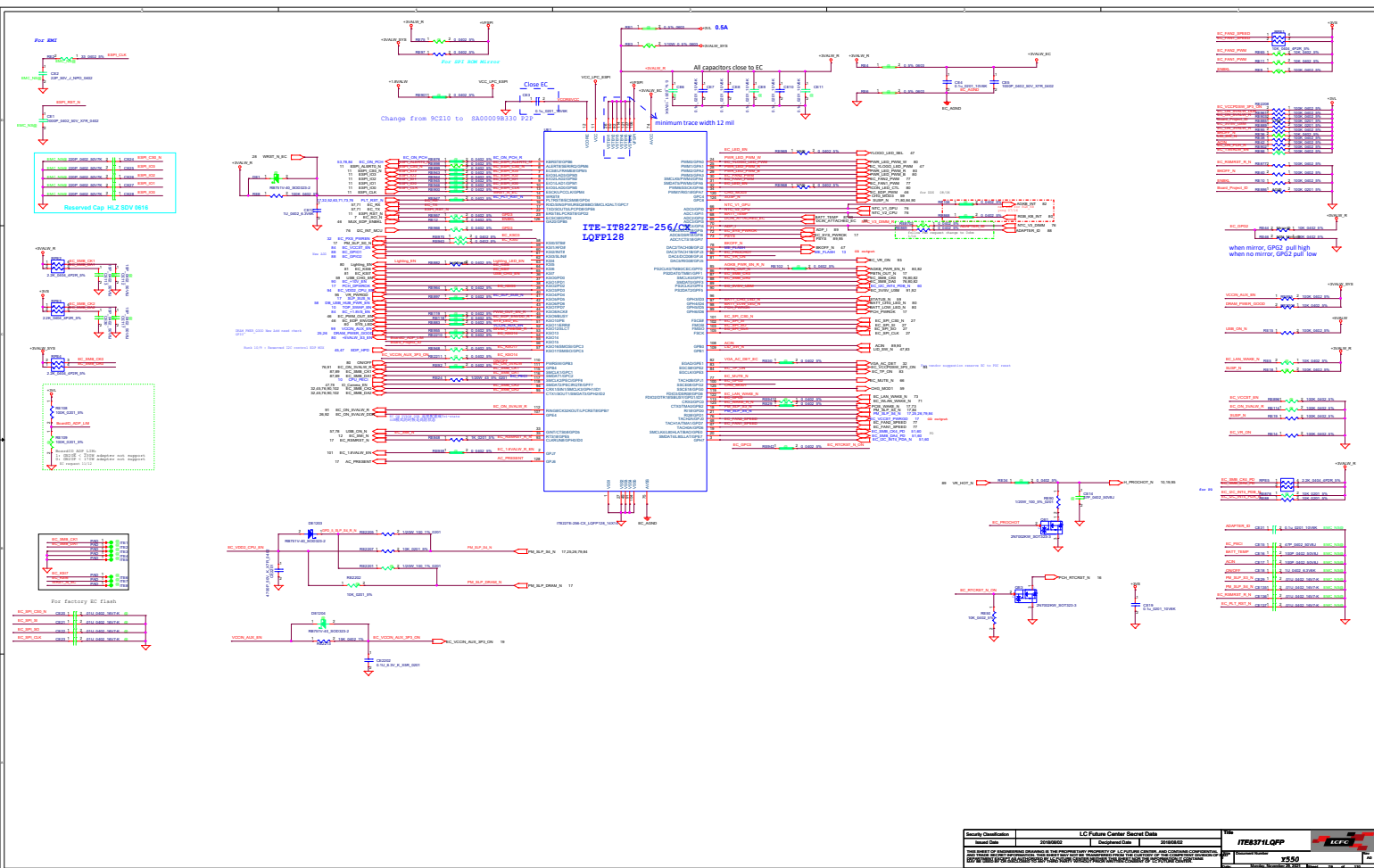
Right Side USB2.0 Port X1 (USB/B)

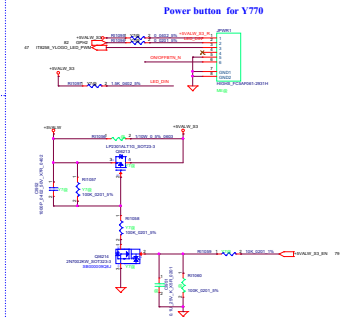
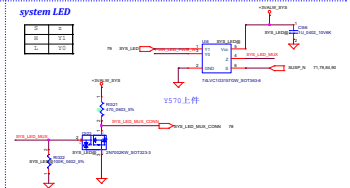
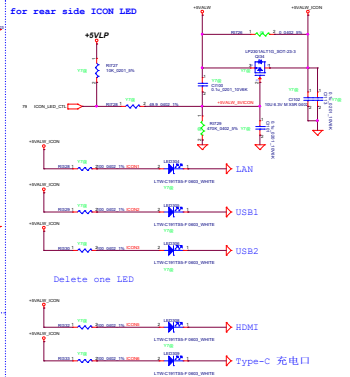
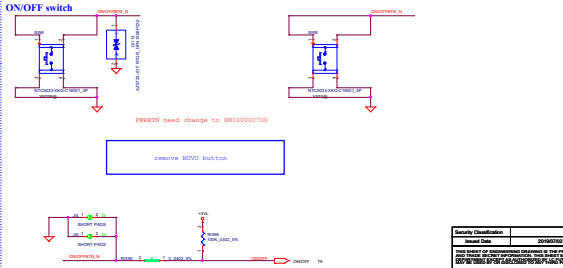
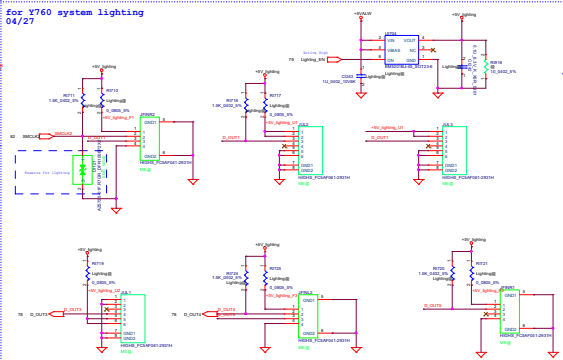
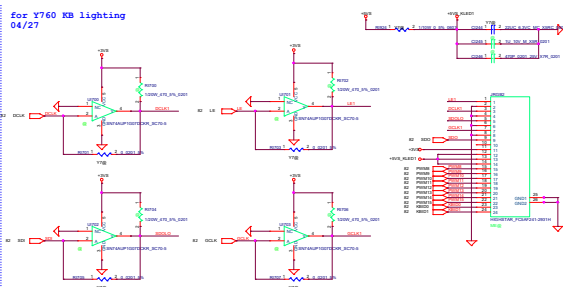
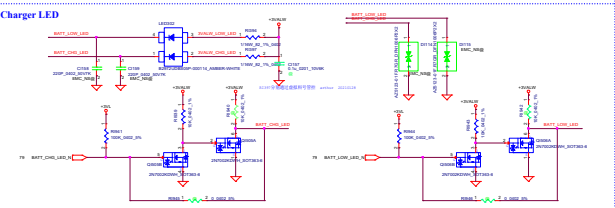
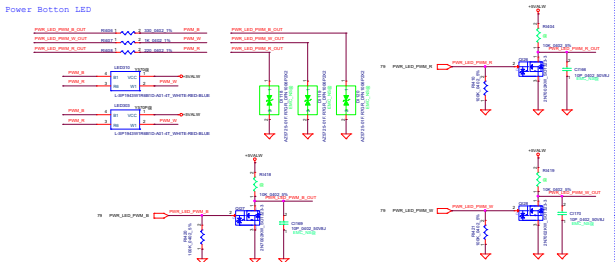
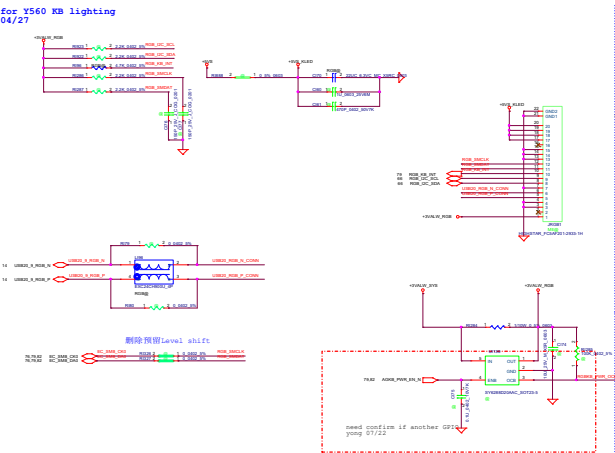


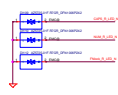
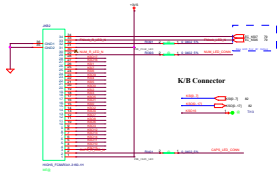
USB3.1 PORT x1



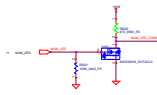
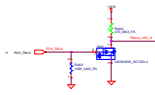
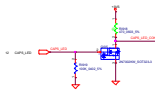
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Issued Date		Decommission Date		Rev	
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Module Number: 28, 2021		118		Date	Sheet #



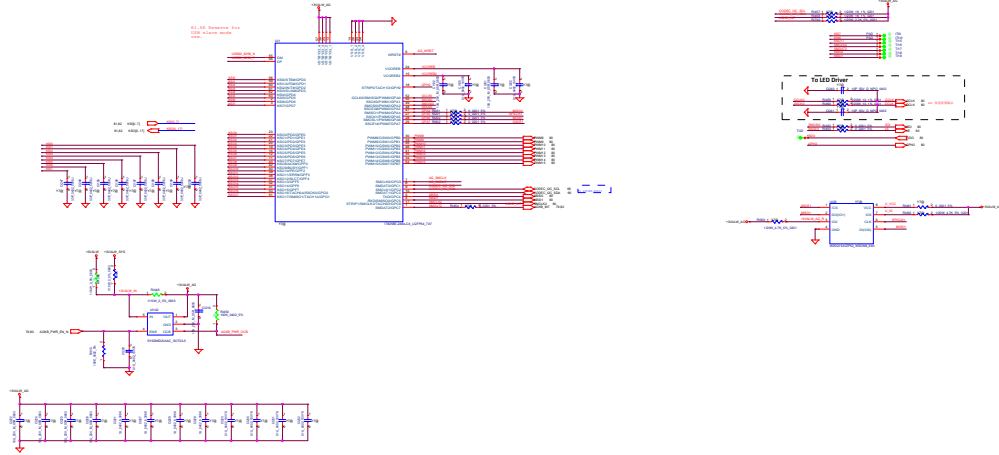




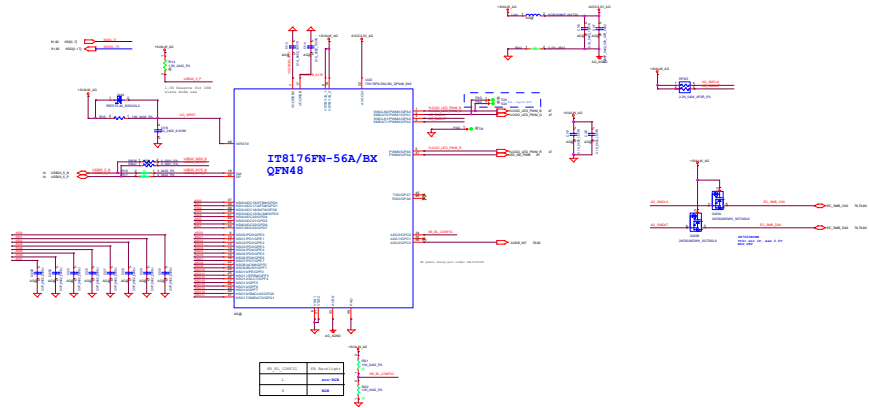
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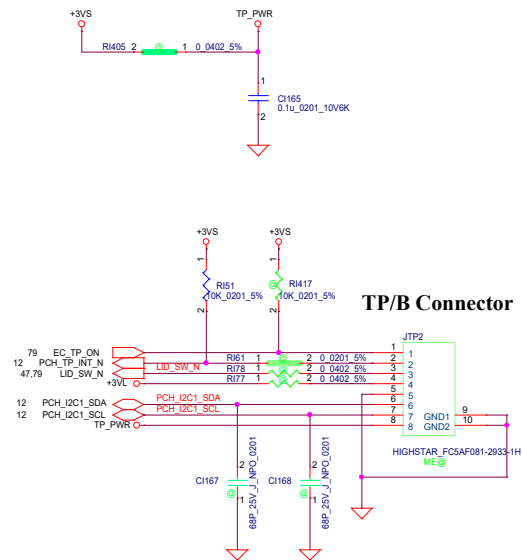
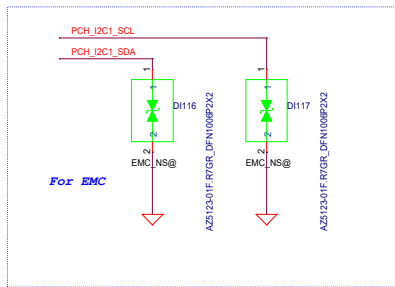
IT8258



IT8176



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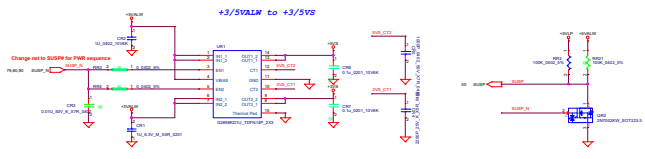


Security Classification	LC Future Center Secret Data	
Issued Date	2018/08/02	Deciphered Date
		2018/08/02

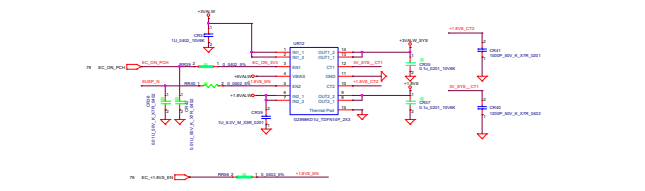
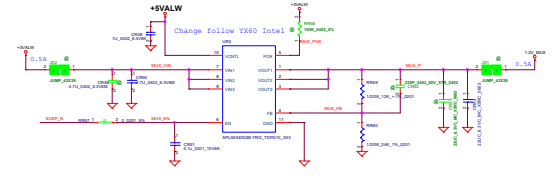
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Title	
KBD/PWR/IO/LED/TP Conn.	
Size	Document Number
B	Y550
Date:	Monday, November 28, 2021

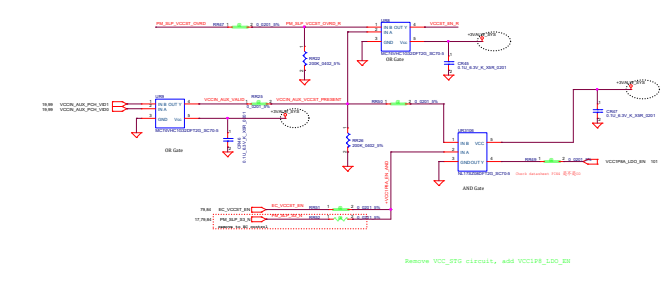
Rev	
AD	
Sheet	83 of 110



For Parade 1.2V

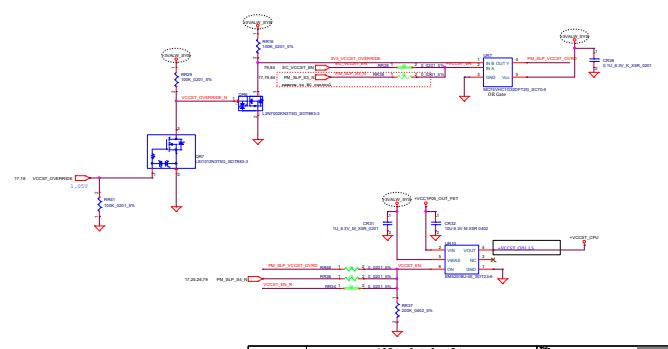



For +VCCP08N_3F3

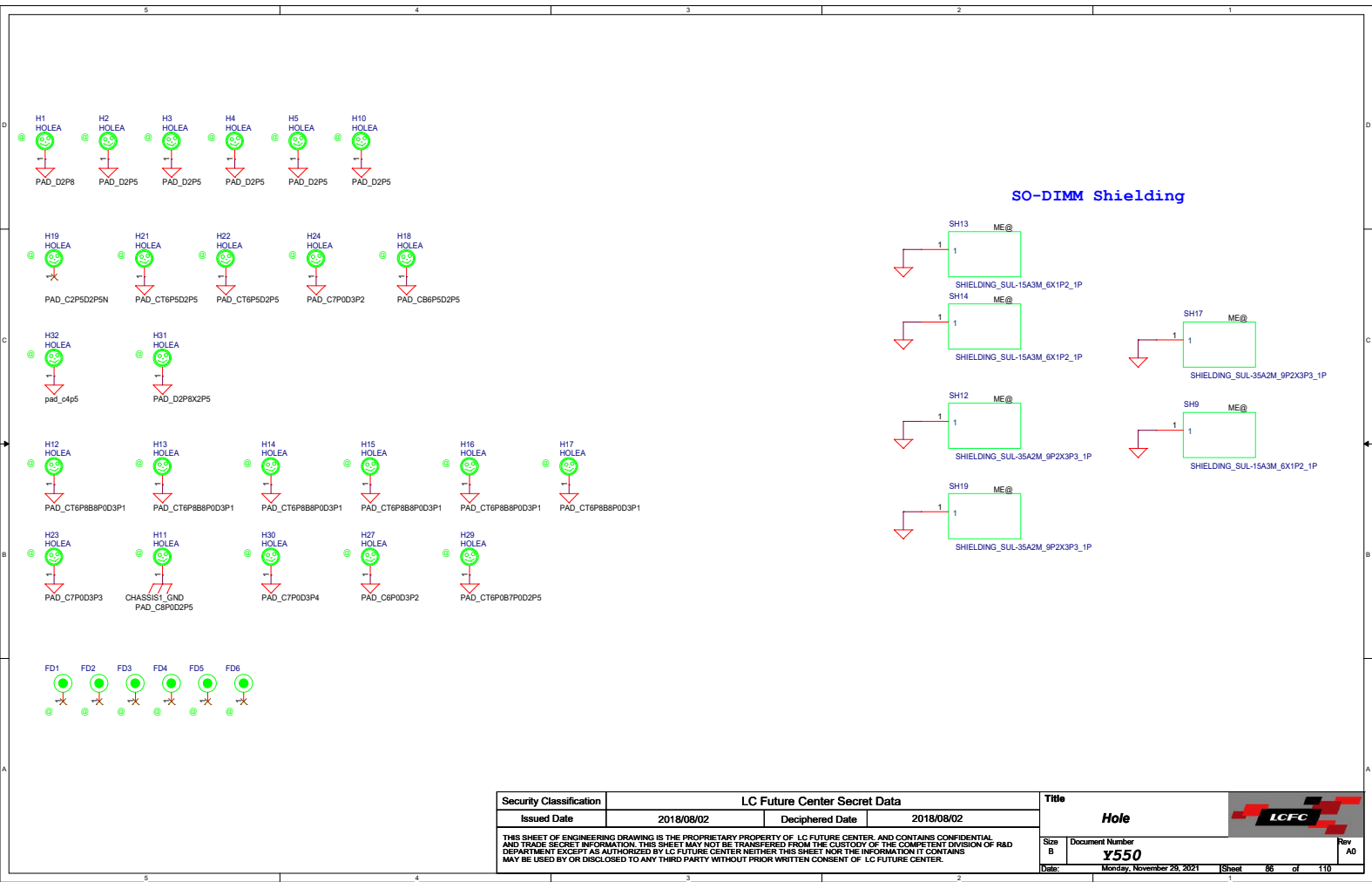


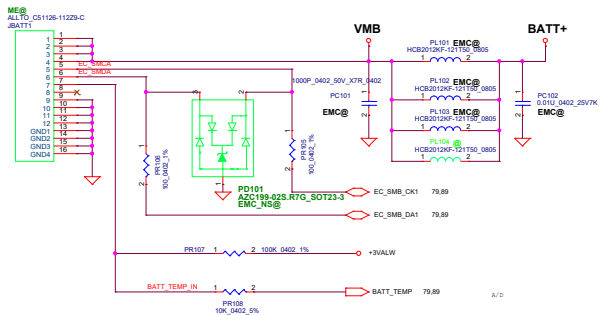
Remove VCC_0V0 circuit, add VCCP08N_3F3

VCCP08N_3F3

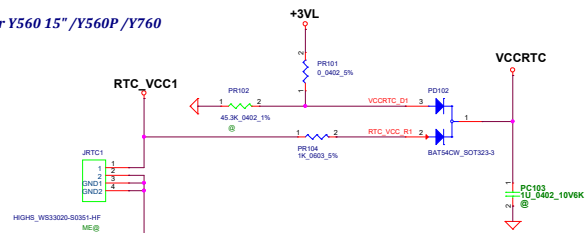



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Issued Date	2019/11/06	Deciphered Date	2019/11/05	Yx60 TGL-H		
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Date: Monday, November 29, 2021				Sheet 85 of 110		Rev A0

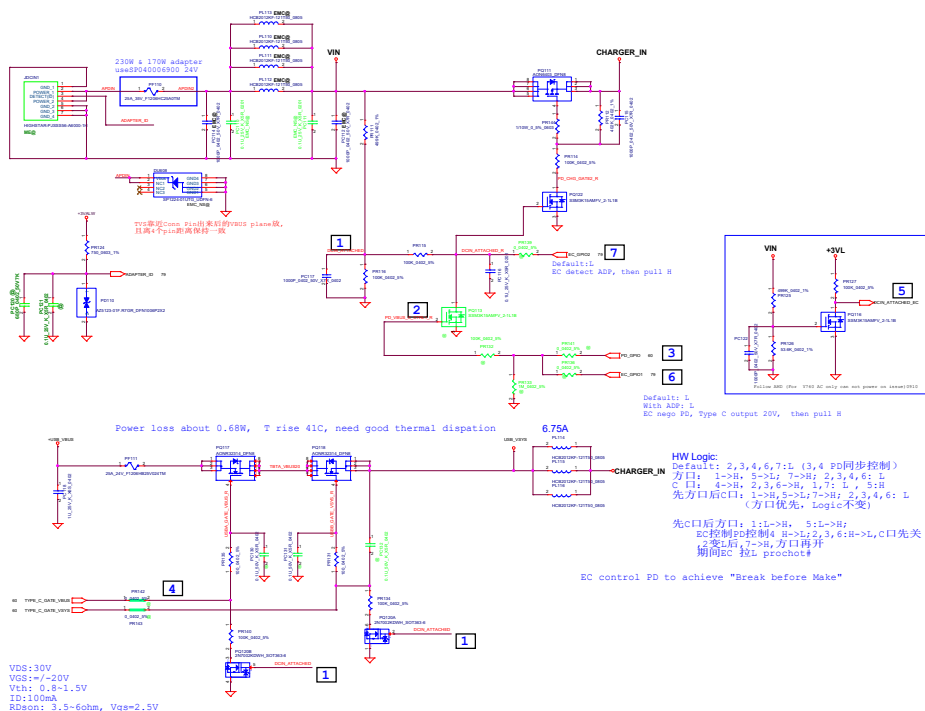




For Y560 15"/Y560P/Y760



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Issued Date		Deciphered Date		PWR_DCIN/RTC	
2018/08/02		2018/08/02			
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Size		Document Number		Rev	
5		Y560 AMD		A0	
Date		Monday, November 26, 2021		Sheet 87 of 110	



ACDET Threshold:min:17.878V
BAT Max V=17.6V

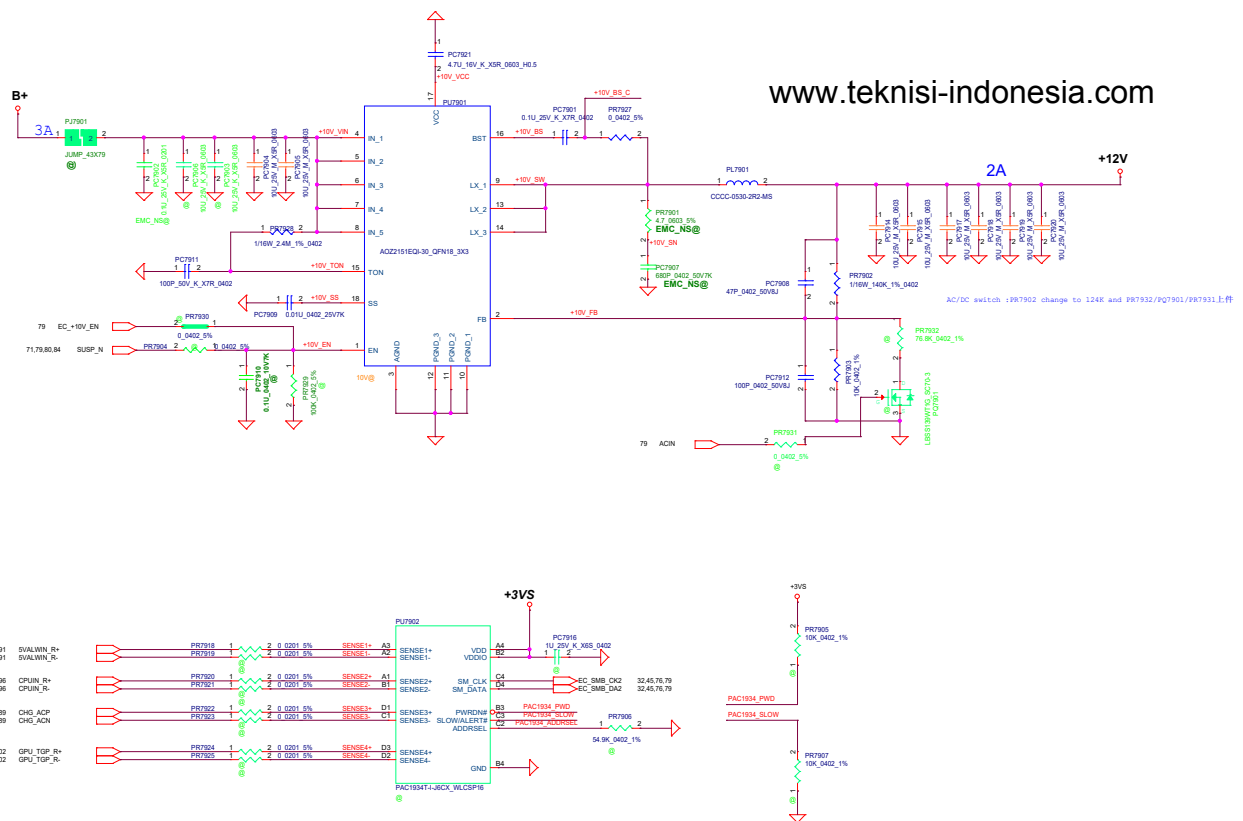
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PR5415=15K 0.75V=100W

IchargeLIM=17.6A
IchargeLIM=70.4A

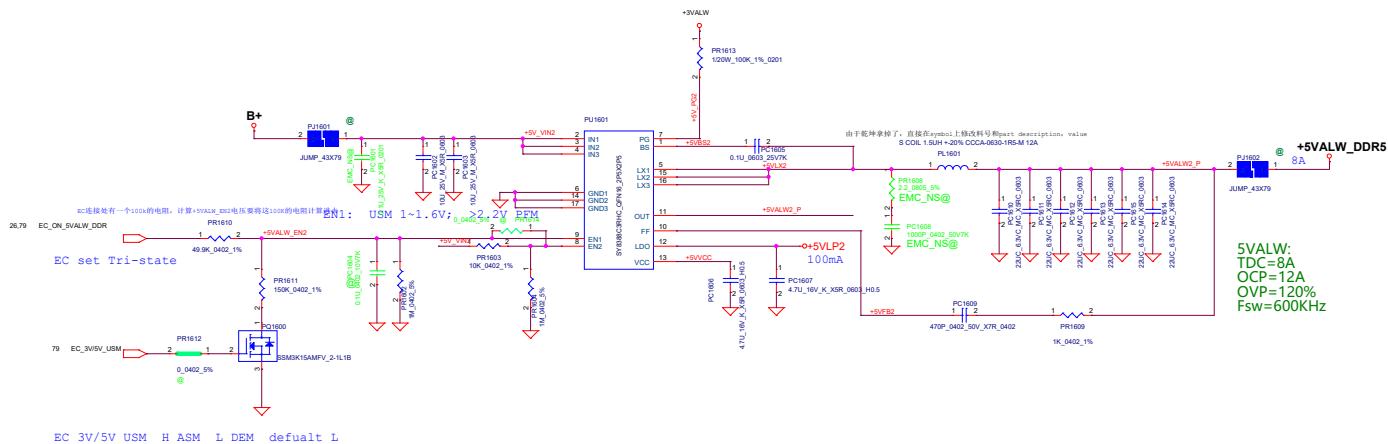
For Charge current ~16A


V charge (MAX):17.6V
I charge (MAX):16A
FSW:500K

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Issued Date	2018/08/02	Disphanded Date	2018/08/02	PWR-charger	
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Doc Number	Y550	Rev	01	Material	2018.08.02



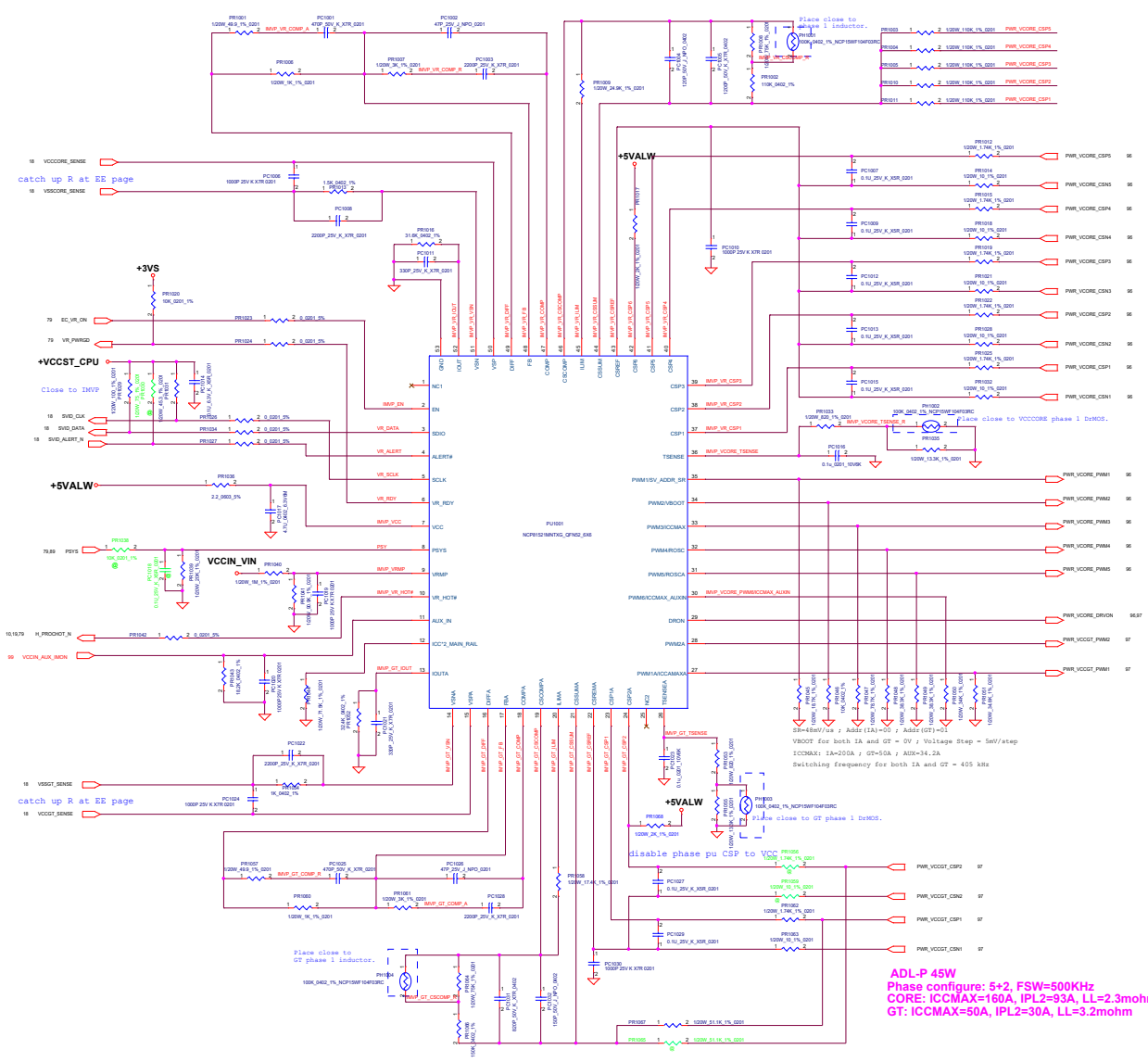
Security Classification		LC Future Center Secret Data		Title	
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Size	Code	Document Number	Y360 AMD		
Date	Version	Revision	2021	10/2021	110



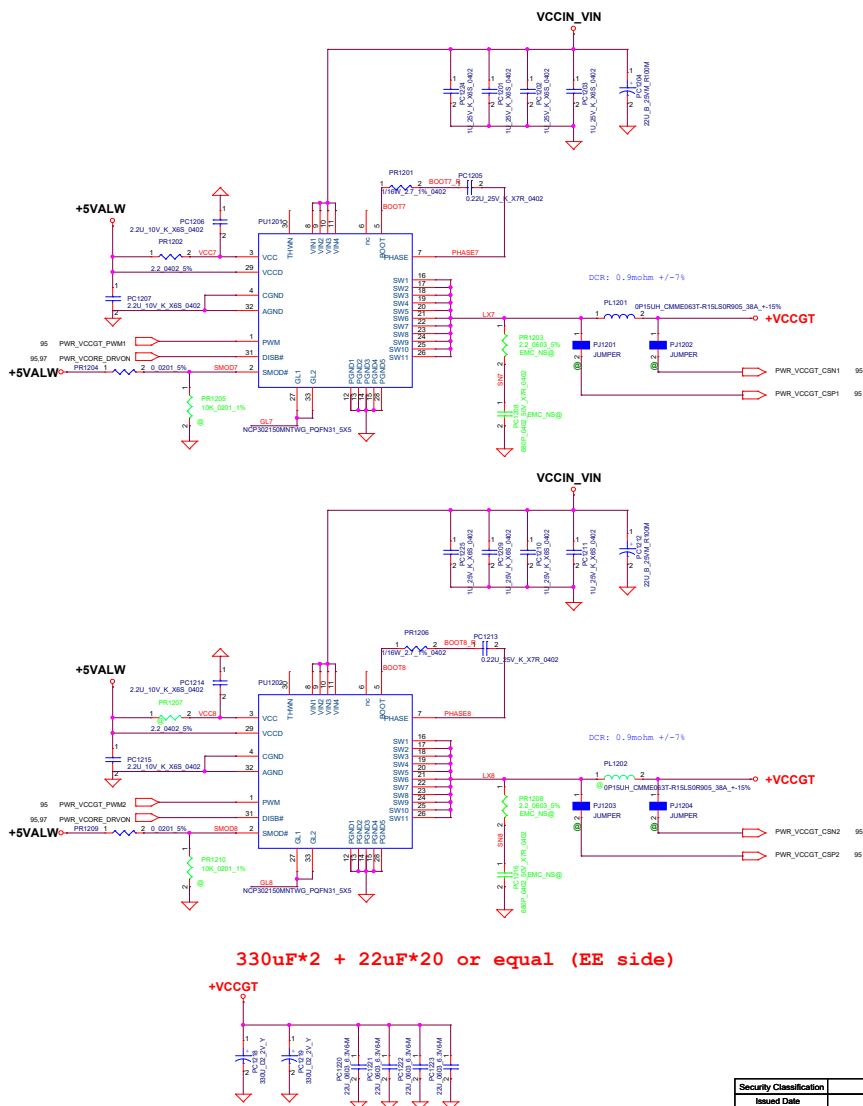
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Issued Date	2019/07/02	Deciphered Date	2019/07/02	PWR_Memory PWR	
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				Rev	00
Date				Monday, November 28, 2017	Sheet 93 of 118



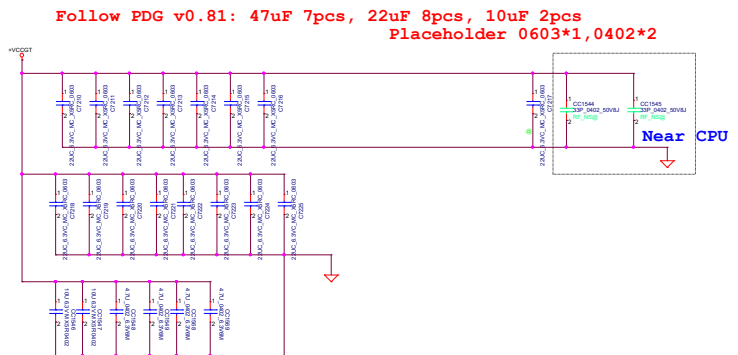
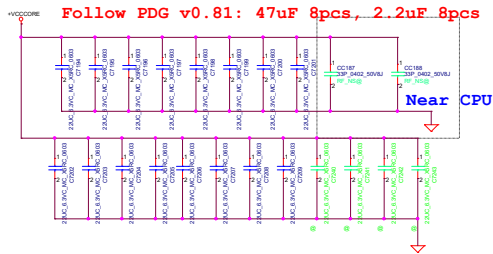
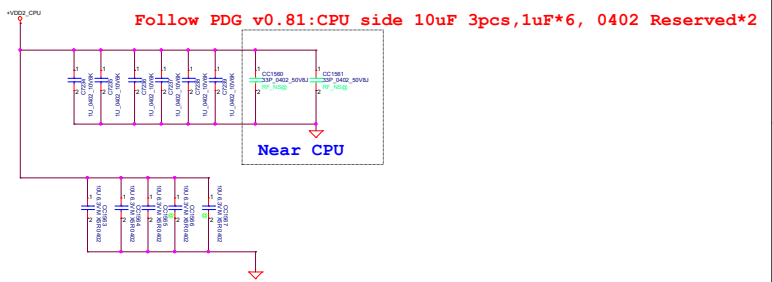
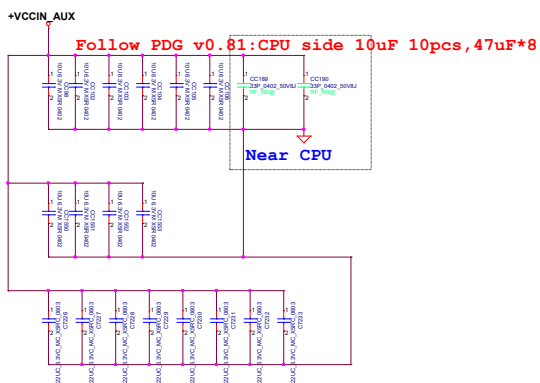


ADL-P 45W
Phase configure: 5+2, FSW=500KHz
CORE: ICCMAX=160A, IPL2=93A, LL=2.3mohm
GT: ICCMAX=50A, IPL2=30A, LL=3.2mohm

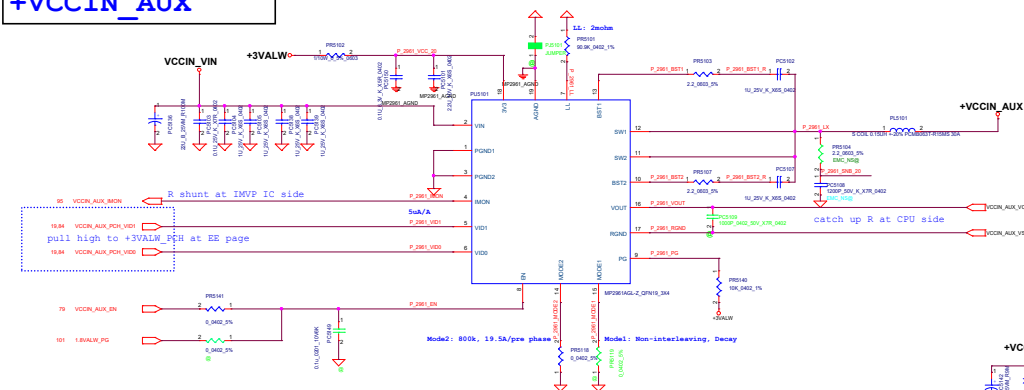


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Issued Date		Deciphered Date		Change Lise_PWR	
2018/08/02		2018/08/02			
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March 29, 2021					

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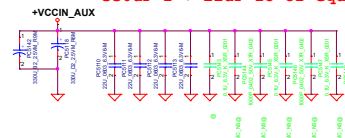
STATE	Interleaving	VFD down option	Resistor to ON
M1	0	slow down	0
M2	1	slow down	50k
M3	1	brake	150k
M4	0	brake	>100k or float

State	Fx	GWR	Indicator to B
s0	00000	000	0
s0	10000	000	000
s0	00000	070	1000
s0	00000	070	0000 as 0000

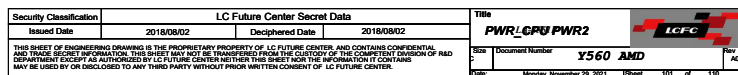
STATE	Load line	Registered to USD
NC	1000k	0
NC	1.5000k	90k
NC	2000k	150k

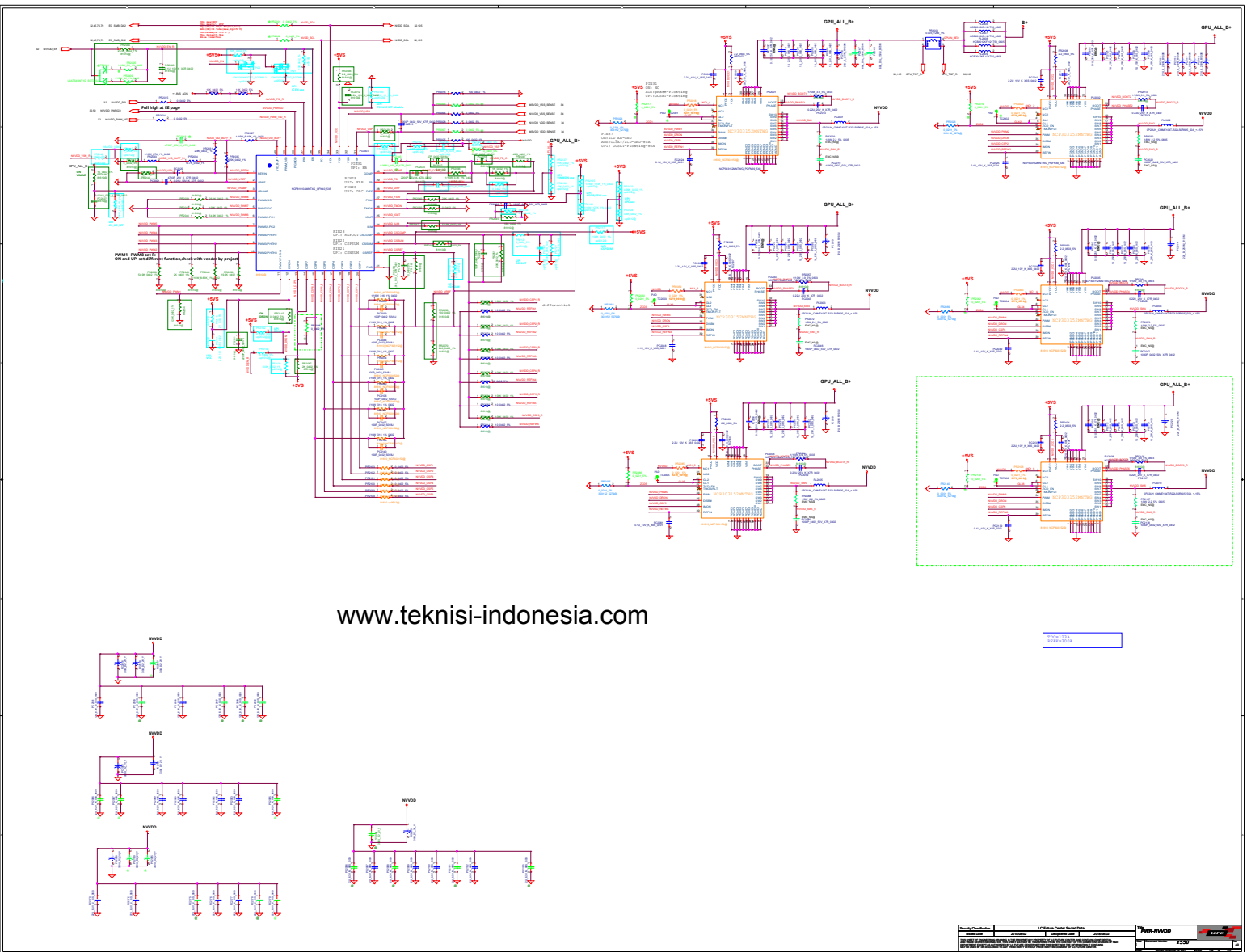
var1	var2	var3 (v)
0	0	0
0	1	1.1
1	0	1.45

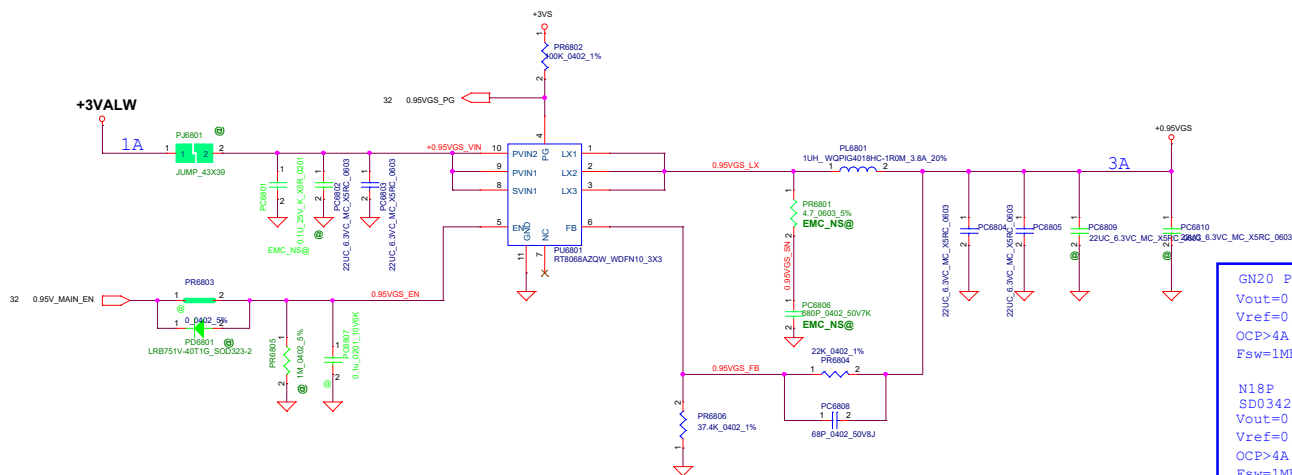
330uF*1 + 22uF*18 or equal (EE side)



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Issued Date	2018/08/02	Deciphered Date	2018/08/02	Size	Document Number
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				Rev	A0
				Date	Monday, November 26, 2021







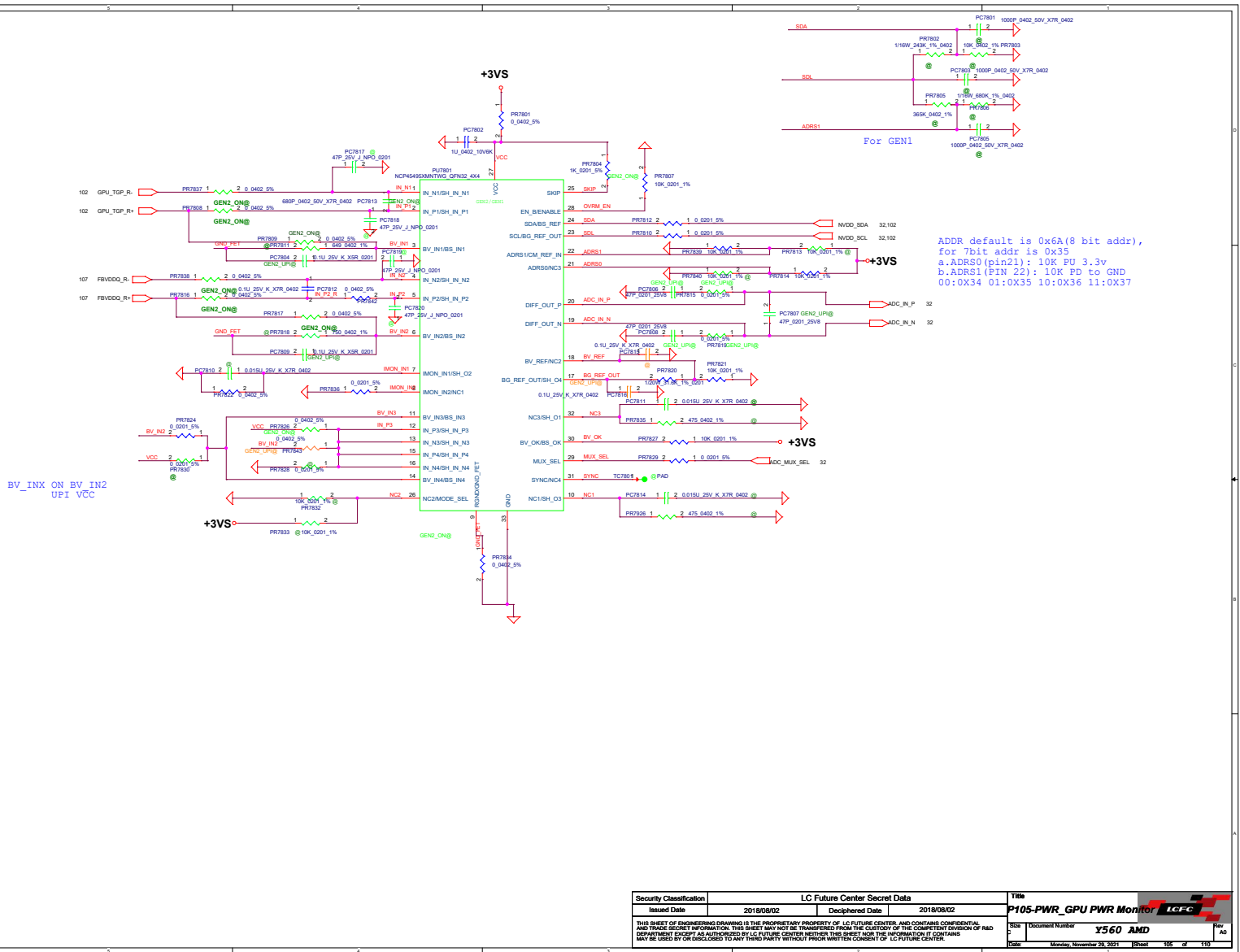


GN20 PR6804=22K
 Vout=0.953V±3%
 Vref=0.6V
 OCP>4A
 Fsw=1Mhz

 N18P PR6804=26.1K
 SD03426128J
 Vout=0.953V±3%
 Vref=0.6V
 OCP>4A
 Fsw=1Mhz

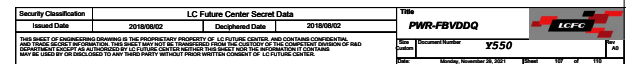
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Issued Date	2018/08/02	Deciphered Date	2018/08/02	PWR_GPU PWR	
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Issued Date	2018/08/02	Deciphered Date	2018/08/02	PWR_GPU PWR2		
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Issued Date	2018/08/02	Deciphered Date	2018/08/02	GPU PWR Decoupling			
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<div><div>Issue</div><div>Monday, November 26, 2021</div></div> <div><div>Sheet</div><div>108 of 110</div></div>				



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Date				Monday, November 26, 2021
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Security Classification	LC Future Center Secret Data		Title			
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				Date	Revised: November 25, 2021	Sheet 119 of 119